TABOR ELECTRONICS

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Proteus Series Arbitrary Waveform Generator/ Transceiver Module User Manual

Rev. 1.3

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Document Revision History

Revision	Date	Description	Author
1.3	11-Mar-2024	• Release supporting WDS 1.7.050 or higher, SCPI Rev. 1.136, FPGA version 237 or higher. • 1.2 Related Documentation – New. • Table 2.1 Ordering Information – Added P9482M, and P9484M • Table 2.2 Available Options for Proteus Series Module Platform – Added G1 and G2. • 2.2 Features and Highlights – Updated. • 2.3 System Requirements – Updated. • 2.4 Options – Updated. • 2.5.1 Proteus AWT Front Panel – New. • Table 4.1 Proteus Models vs. GS/s – Updated. • Table 4.2 Waveform Sampling Rate Range vs. DAC Sampling Rate as a Function of the Interpolation Factor – New. • 6.3 Task Table Parameters – New parameter Trigger ADC. • 8 DUC Operation – New. • 10 Digitizer – New. • 12 Proteus Module Specifications – Updated.	Joan Mercado Jakob Apelblat
1.2	05-Apr-2021	• 1.3 Software Support – New. • Removed section “Programming”. Refer to Proteus Programming Manual. • Removed sections “Minimum System Requirements” and “Wave Design Installation”. Refer to WDS User Manual. • 12.7 Direct Output – Changed amplitude from “600 mVpp” to “1 mVpp to 550 mVpp”.	Jakob Apelblat
1.1	28-Oct-2020	• Changed page size to letter. • 12.16 Digitizer Characteristics (AWT Option) – Changed Acquisition Memory from “<2 GS/channel” to “Up to max memory size” • Removed WDS description and replaced it with a reference to the WDS User Manual. • 9.6.2 Internal Trigger – New note. • 12 Proteus Module Specifications – Minor formatting. • 14 Appendix Log File – New.	Jakob Apelblat

Revision	Date	Description	Author
1.0	15-Jul-2020	• Original release supporting WDS version 1.2.192, FPGA version 1.2.0	Jonathan Netzer

Acronyms & Abbreviations

Acronym	Description
µs or us	Microseconds
ADC	Analog to Digital Converter
AM	Amplitude Modulation
ASIC	Application-Specific Integrated Circuit
ATE	Automatic Test Equipment
AWG	Arbitrary Waveform Generators
AWT	Arbitrary Waveform Transceiver
BNC	Bayonet Neill–Concelm (coax connector)
BW	Bandwidth
CW	Carrier Wave
DAC	Digital to Analog Converter
dBc	dB/carrier. The power ratio of a signal to a carrier signal, expressed in decibels
dBm	Decibel-Milliwatts. E.g., 0 dBm equals 1.0 mW.
DDC	Digital Down-Converter
DHCP	Dynamic Host Configuration Protocol
DSO	Digital Storage Oscilloscope
DUC	Digital Up-Converter
ENoB	Effective Number of Bits
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
EW	Electronic Warfare
F_{NCO}	Numerically Controlled Oscillator Frequency
FPGA	Field-Programmable Gate Arrays
GHz	Gigahertz
GPIB	General Purpose Interface Bus
GS/s	Giga Samples per Second

Acronym	Description
GUI	Graphical User Interface
HP	Horizontal Pitch (PXIe module horizontal width, 1 HP = 5.08mm)
Hz	Hertz
IF	Intermediate Frequency
I/O	Input / Output
IP	Internet Protocol
IQ	In-phase Quadrature
IVI	Interchangeable Virtual Instrument
JSON	JavaScript Object Notation
kHz	Kilohertz
LCD	Liquid Crystal Display
LO	Local Oscillator
MAC	Media Access Control (address)
MDR	Mini D Ribbon (connector)
MHz	Megahertz
MIMO	Multiple-Input Multiple-Output
ms	Milliseconds
NCO	Numerically Controlled Oscillator
ns	Nanoseconds
PC	Personal Computer
PCAP	Projected Capacitive Touch Panel
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PRBS	Pseudorandom Binary Sequence
PRI	Pulse Repetition Interval
PXI	PCI eXtension for Instrumentation
PXIe	PCI Express eXtension for Instrumentation
QC	Quantum Computing
Qubits	Quantum bits
RADAR	Radio Detection And Ranging
R&D	Research & Development

Acronym	Description
RF	Radio Frequency
RT-DSO	Real-Time Digital Oscilloscope
s	Seconds
SA	Spectrum Analyzer
SCPI	Standard Commands for Programmable Instruments
SFDR	Spurious Free Dynamic Range
SFP	Software Front Panel
SMA	Subminiature version A connector
SMP	Subminiature Push-on connector
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
TFT	Thin Film Transistor
T&M	Test and Measurement
TPS	Test Program Sets
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VCP	Virtual COM Port
Vdc	Volts, Direct Current
V p-p	Volts, Peak-to-Peak
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
WDS	Wave Design Studio

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1 General

1.1 Scope

The scope of this manual is to describe the setup and operating procedures of the Tabor Electronics Proteus series module platform.

1.2 Related Documentation

- Wave Design Studio User Manual
- Proteus Programming Manual
- Proteus Series Performance Verification Manual
- Proteus DUC Primer
- Proteus AWT Radar Primer
- Qubit Characterization (IEEE Applications Note)
- Direct Generation/Acquisition of Microwave Signals
- Effective Number of Bits for Arbitrary Waveform Generators

1.3 Software Support

The **Wave Design Studio (WDS)** is a software package that enables full control and programming of your Tabor Electronics device via a user-friendly graphical user interface. Use the **TE Update Tool** to update the Proteus device FPGA. The programs and the user manual can be downloaded from the Tabor Electronics website at http://www.taborelec.com/downloads.

1.4 Document Conventions

1.4.1 General

Convention	Description	Example
Bold Writing	Indicates an item/message in the User Interface.	Click the **On** button.
<Angled and Bolded Brackets>	Indicates a physical key on the keyboard.	Press <Ctrl>+<B>.

Caution!
A Caution indicates instructions, which, if not followed, may result in damage to the equipment or to the loss of data.

Note

A note provides additional **information** to help obtain optimal equipment performance.

Idea
An idea provides an alternate procedure to obtain the same results.

1.5 Safety

To avoid electrical shock, fire or personal injury:

- Use only the proper power cord and certified for the country of use.
- This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, the grounding conductor must be connected to the ground. Before connecting to the power input or output, ensure that the product is properly grounded.
- Do not operate this product with removed covers or panels.
- Observe all the ratings and markings on the product. Search this manual for further rating information, before connecting to it. Do not apply potential that is higher than the maximum rating.
- Do not operate in dark or wet conditions.
- Do not operate in an explosive environment. Keep product clean and dry.

1.6 Maintenance

1.6.1 Preventive Maintenance

There are no hardware adjustments within Proteus Generators. Tabor Electronics Ltd., recommends that the Proteus Generator is calibrated every 24 months or whenever a problem is suspected. The specific calibration interval depends upon the accuracy required. No periodic preventive maintenance is required.

1.6.2 Long Term Storage or Repackaging For Shipment

If the instrument is to be stored for a long period of time or shipped immediately, proceed as directed below. If you have any questions, contact your local Tabor Electronics representative or the Tabor Electronics Customer Service Department.

1. Repack the instrument using the wrappings, packing material and accessories originally shipped with the unit. If the original container is not available, purchase replacement materials.
2. Be sure the carton is well sealed with strong tape or metal straps.
3. Mark the carton with the model and serial number. If it is to be shipped, show sending and return address on two sides of the box.
4. If the instrument is to be shipped for service or repair, the following information must be included with the shipment:

- Name and address of the owner.

- Record the model and serial number of the instrument, options, and firmware version.
- Note the problem and symptoms – detailed information will help in verifying the problem
  - What was the instrument setup, such as the run mode, arbitrary/task mode, task table etc.
  - Did the unit work; then fail or was it dead on arrival.
  - What other equipment was connected to the generator when the problem occurred, such as external trigger or clock.
- The name and telephone number of someone familiar with the problem who can be contacted by Tabor Electronics if any further information is required.
- Show the returned authorization order number (RMA) as well as the date and method of shipment.

Note

Always obtain a return authorization number from the factory before shipping the instrument to Tabor Electronics.

2 Introduction

2.1 Overview

This manual provides a detailed functional description for the Tabor Electronics Proteus series module platform. Proteus is a series of arbitrary waveform generators and transceivers that transmit, receive and perform digital signal processing all in a single instrument with various form-factors and sampling rate options. The Proteus module is PXIe-based (PCI Express eXtension for Instrumentation) to be plugged into a standard PXIe chassis such as the Tabor PXE21100, 21 slot PXIe chassis. The manual covers the following models listed in the below ordering information. For a list of options refer to Table 2.2 Available Options for Proteus Series Module Platform.

Table 2.1 Ordering Information

Model	Description
P1282M	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, module RF AWG
P1284M	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, module RF AWG
P2582M	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, module RF AWG
P2584M	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, module RF AWG
P9082M	9 GS/s, 8 bit, 4 GS memory, 2 channels, 8 markers, module RF AWG
P9482M	9 GS/s, 16 bit, 8 GS memory, 2 channels, 8 markers, module RF AWG
P9484M	9 GS/s, 16 bit, 8 GS memory, 4 channels, 8 markers, module RF AWG

Note
P2582M = **P** (Model = Proteus) + **258** (Sampling Rate = 25E08 = 2.5E9) + **2** (# channels = 2) + **M** (Platform = Module)

Figure 2.1 Proteus Model P2584M

Figure 2.2 Proteus Model P9484M-AWT

2.2 Features and Highlights

- Dual or four channel 1.25 GS/s & 2.5 GS/s, 16-bit, or dual channel 9 GS/s, 8-bit, AWG & AWT (Arbitrary Waveform Generator/Transceiver) configurations
- Four channels 9GS/s 16 bit, AWG & AWT configurations (P9482M, P9484M).
- Integrated NCO (Numerically Controlled Oscillator) for digital upconverting to microwave frequencies
- Real time data streaming directly to the FPGA for continuous and infinite waveform generation
- 8 GHz bandwidth, 5.4 GS/s 12-bit digitizer option for feedback control system and conditional waveform generation
- Innovative task-oriented sequence programming for maximum flexibility to generate any imaginable scenario
- Up to 16 GS waveform memory with the ability to simultaneously generate and download waveforms
- Excellent phase noise and spurious performance
- User customizable FPGA block for real time processing and application specific functionality
- High speed PCIe GEN3 x8 lanes communication interface

- Modular and space efficient PXIe (PCI Express eXtension for Instrumentation) platform, easily scalable to hundreds of channels

2.3 System Requirements

The following is required to operate Proteus:

- PXIe compatible chassis
- PC with Windows 10 operating system

2.4 Options

The Proteus series module platform is a dual-slot PXIe arbitrary waveform generator and can be ordered with the following options.

Table 2.2 Available Options for Proteus Series Module Platform

Option	Description	Model
4M1	4 GS memory	P1282M, P2582M
4M2	4 GS memory	P1284M, P2584M
8M1	8 GS memory	P1282M, P2582M
8M2	8 GS memory	P1284M, P2584M, P9082M
16M1	16 GS memory	P9082M
DO1	9 GHz BW direct (DAC) output	P1282M, P2582M
DO2	9 GHz BW direct (DAC) output	P1284M, P2584M, P9082M
DC1	DC output for IQ baseband applications	P9482M
DC2	DC output for IQ baseband applications	P9484M
DJ1	Dynamic jump input option, occupies an additional slot	P1282M, P2582M, P9482M
DJ2	Dynamic jump input option, occupies an additional slot	P1284M, P2584M, P9082M, P9484M
LVTTL1	LVTTL marker output	P128xM, P258xM, P9082M, P948xM
MRK1	4 extra markers, occupies an additional slot	P1282M, P2582M, P9482M
MRK2	8 extra markers, occupies an additional slot	P1284M, P2584M, P9082M, P9484M
LTJ1	Ultra-low trigger jitter	P1282M, P2582M, P9482M
LTJ2	Ultra-low trigger jitter	P1284M, P2584M, P9082M, P9484M
G1	Low waveform granularity	P1282M, P2582M, P9482M

G2	Low waveform granularity	P1284M, P2584M, P9082M, P9484M
DUC	Digital up-converter for models	P2582M, P2584M
TRG	Faster trigger input (50 MHz instead of 10 MHz)	All models
AWT	5.4 GS/s single, 2.7 GS/s dual channel 12-bit digitizer, occupies an additional slot	All models
STM	Up to 6 GS/s streaming option depending on model	All models
PROG	FPGA programming capability with built-in demodulation and digital filters	All models
Shell	Integration to allow simple FPGA control and programming	All models
PXE21100	21 slot PXIe chassis	All models
PXE6410	6 slot PXIe chassis with an embedded PC	All modules

Option M – This option offers to increase the standard waveform memory of the unit as detailed in the table below:

Table 2.3 Memory Configuration and Options

Model	Standard	4M1	4M2	8M1	*8M2	16M1
P1282M	1GS	4GS		8GS		
P1284M	1GS		4GS		8GS	
P2582M	2GS	4GS		8GS		
P2584M	2GS		4GS		8GS	
P9082M	4GS				8GS	16GS

Option DO – There are two available output configurations:

1. Direct Output (DO): This is a direct AC coupled output without an amplifier and is optimized for maximum analog BW as well as best SFDR (Spurious Free Dynamic Range). It offers a programmable amplitude range of 1mVpp to 550 mVpp.
2. DC Output: This is the default configuration. A DC coupled output amplifier offering up to 1.3 Vpp with a voltage window of ±1.15 V.

Note
The P948xM comes with DO as default.

Option DJ – This option offers the capability of switching segments through an external MDR connector. The MDR connector occupies an additional PXI slot. Refer to 13 Appendix A. MDR Interface for a pin description.
Option MRK – This option adds a digital markers card, with 8 additional markers and occupies an extra PXI slot.
Option LVTTL – This option LVTTL marker output (replaces the 1.3Vpp default markers).
Option LTJ – This option improves the Proteus trigger jitter to SQRT(SCLK period^2 + 150e-12^2).

Option G – This option increases the segment resolution for segments that are both fast and short. In the case of the P9082M the segment resolution, for the first 128 segments that are shorter than 8kpts, is increased to 32 points. For the P128xM, P258xM and P948XM, the segment resolution, for the first 128 segments that are shorter than 4kpts, is increased to 16 points.
Option AWT – This option transforms the Proteus to an arbitrary waveform transceiver with the capability of both generating and receiving signals. The option adds a 2.7 GS/s dual channel or 5.4 GS/s single channel digitizer card allowing to complete a fully closed loop system controlled by a single FPGA. With this option the Proteus AWT occupies 3 PXIe slots.
Option PROG – This option enables the user to use built in digital processing library blocks such as demodulators, filters and math functions as part of the signal processing chain without FPGA programming knowledge.
Option Shell – This option is for users with advanced FPGA programming knowledge in Xilinx Vivado Design Suite. The Proteus is supplied only with the necessary communications and data transfer cores and enables the user to implement their own IP on the available resources of the FPGA.
The options depicted below require an additional PXIe slot.

Figure 2.3 P9802M-AWT

2.5 Front Panel

The front panel of the Proteus device varies according to the device model and configuration. However, regardless of the configuration, all connector types follow the same principle. All high-frequency analog output and input connectors are of SMA type. All low-frequency analog output

and input connectors as well as all digital output and input connectors are of SMP type. In addition, there is a “STATE” LED to indicate if there is any problem with the device.
Below is the front panel of the P2584M model:

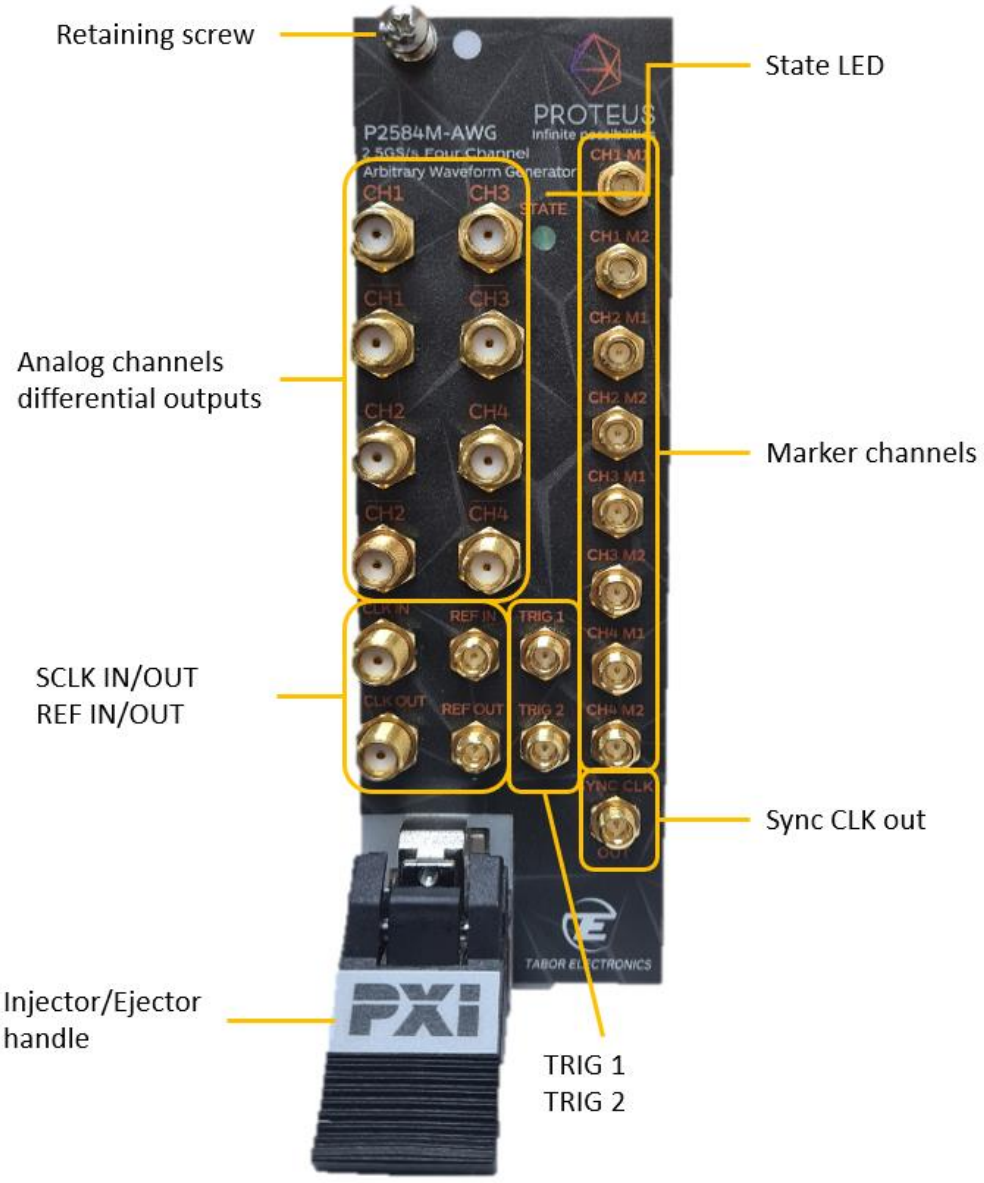

Figure 2.4 P2584M Front Panel

- **Retaining Screw –** The retaining screw is used to secure the module to the PXIe chassis.
- **CH1/2/3/4 –** There are two SMA connectors for each channel output, normal (top) and inverted (bottom) outputs. The output source impedance is 50 Ω (100 Ω when connected differentially) therefore the cable connected to this output should be terminated with a 50 Ω load resistance. For different load resistance, determine the actual amplitude from the following equation:

$$V_{out} = 2V_{prog}\left(\frac{R_{load}}{50 + R_{load}}\right)$$

The output amplitude is doubled when the load impedance is above roughly 10 kΩ. Also, the output can be turned on and off. However, turning the output off stops the signal, but leaves low impedance on the output terminals.

Note

When using the outputs as single ended it is necessary to use a 50 Ω termination on the inverted output to prevent any distortion on the output signal.

- **CLK IN –** The sample clock in SMA connector accepts an external signal that will replace the internal sample clock generator. This input, accepts signals covering the instrument's entire sample clock range, with an input level range of 0 V to 1 V. The output impedance of this connector is 50 Ω and it is AC coupled. The sample clock input is active only after selecting the external SCLK source option.
- **CLK OUT –** The sample clock out SMA connector outputs the internal sample clock generator or the external SCLK if an external sample clock is used. The sample clock out signal covers the entire sample clock range, with an output amplitude of 0.5 V to 1 V depending on the frequency. The output impedance of this connector is 50 Ω and it is AC coupled.
- **REF IN –** The reference in SMP connector accepts signals of either 10 MHz or 100 MHz. This input is normally used for synchronizing system components to a single clock reference. The Proteus device must be programmed to the reference frequency value and placed in external reference mode before it will use this input as reference.
- **REF OUT –** The reference out SMP connector outputs the 100M Hz internal reference (square waveform) or if using an external reference, the Ref Out outputs the external reference frequency. This output can be used to synchronize other system components to the Proteus clock reference.

Module Synchronization

When synchronizing multiple modules, the modules need to be daisy chained between REF OUT to REF IN. Therefore, in this mode the REF OUT is not available and is used for synchronization. The REF IN of the master unit can accept an external reference signal, and this will be the reference for all modules.

- **STATE –** System status LED.
  - **Solid Green** – Normal operation.
  - **Off –** System fault. Contact Tabor Electronics.

- **TRIG 1/2 –** In general, the trigger inputs are used to initiate or abort waveform generation. In arbitrary mode this is used to start or stop a current segment from playing. In task mode this can also be used as a condition signal for how to progress in the task table. The trigger input is inactive when the generator is in continuous operating mode. When placed in trigger mode, the trigger input is made active and waits for the right condition to trigger the instrument. Trigger level and edge rising/falling edge are programmable for the trigger input. For example, if your trigger signal rides on a DC level, you can offset the trigger level to the same level as your trigger signal, thus assuring the correct threshold for the trigger signal. The trigger level is adjustable from -5 V to +5 V. The programmed trigger level is common for all channels. All other trigger parameters including trigger state, are independent and can be programmed per channel. The two trigger input connectors are of SMP type. By default, the input impedance is 50 Ω but can be factory configured to 10 kΩ when ordered.
- **CH1-4 M1/2 –** There are between 1 to 4 output markers available for each analog channel output depending on the Proteus model. The markers are generated through SMP connectors and are marked with the channel number they are associated to, and the marker number e.g. CH1 M1 is Marker 1 of Channel 1. Markers can be programmed from remote to create complex digital patterns. Waveform data and marker data are downloaded separately; however each waveform segment has a dedicated marker segment of equal length. Markers output has an output impedance of 50 Ω and marker level can be programmed up to 1.2 Vpp.
- **SYNC CLK –** This SMP connector outputs a clock signal, that is a division of the device sampling clock. For the 9 GS/s Proteus models the sampling clock is divided by 32 and for all other models it is divided by 8. When this signal is used as the sampling clock for an external triggering unit the resulting trigger jitter of the Proteus device will be ~0 ps.

2.5.1 Proteus AWT Front Panel

The front panel of the Proteus AWT (Arbitrary Waveform Transceiver) module occupies three PXIe slots and provides some additional connectors.

Figure 2.5 P9484M-AWT Front Panel

- **CH1/2 IN–** The analog input for the digitizer. There is one SMA connector for each channel input. The input load impedance is 50 Ω.
- **SCLK IN –** The external sample clock for the digitizer. The sample clock in SMA connector accepts an external signal that will replace the internal sample clock generator. This input, accepts signals covering the instrument's entire sample clock range, with an input level range of 0 V to 1 V. The output impedance of this connector is 50 Ω and it is AC coupled. The sample clock input is active only after selecting the external SCLK source option.
- **TRIG IN –** The trigger input is used to initiate the digitizer acquisition. Trigger level and edge rising/falling edge are programmable for the trigger input. For example, if your trigger signal rides on a DC level, you can offset the trigger level to the same level as your trigger signal, thus assuring the correct threshold for the trigger signal. The trigger level is adjustable from -5 V to +5 V. The programmed trigger level is common for all channels. All other trigger parameters including trigger state, are independent and can be programmed per channel. The trigger input connector is of SMA type. By default, the input impedance is 50 Ω but can be factory configured to 10 kΩ when ordered.
- **GPIO1/2 –** For future use.

3 Installation

3.1 Installation Overview

This chapter contains information and instructions necessary to prepare the Proteus device for operation. Details are provided for initial inspection, grounding safety requirements, repackaging instructions for storage or shipment and installation information.

3.2 Unpacking and Initial Inspection

Unpacking and handling of the device requires normal precautions and procedures applicable to handling of sensitive electronic equipment. The contents of all shipping containers should be checked for included accessories and certified against the packing slip to determine that the shipment is complete.

3.3 Safety Precautions

The following safety precautions should be observed before using this product and associated PXIe chassis. Although some instruments and accessories would normally be used with nonhazardous voltages, there are situations where hazardous conditions may be present. This product is intended for use by qualified persons who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. The following sections contain information and cautions that must be observed to keep the device operating in a correct and safe condition.

Caution

For maximum safety, do not touch the product, test cables, or any other instrument parts while power is applied to the circuit under test. ALWAYS remove power from the entire test system before connecting cables or jumpers, installing or removing cards from the chassis. Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always keep your hands dry while handling the instrument.

3.4 Operating Environment

This device is intended for operation within a PXIe chassis as a plug-in module. Ensure the PXIe chassis being used to host the device fully conforms to the latest PXIe specifications, including 3.3 V and 12 V supply rails.
The device is intended for indoor use and should be operated in a clean, dry environment with an ambient temperature within the range of 0°C to 40°C.

Warning

The Proteus device must not be operated in explosive, dusty, or wet atmospheres. Avoid installation of the module close to strong magnetic fields

The design of the device has been verified to conform to EN 61010-1 safety standard per the following limits: Installation (Overvoltage) Category I (Measuring terminals) Pollution Degree 2 Installation (Overvoltage) Category I refers to signal level, which is applicable for equipment

measuring terminals that are connected to source circuits in which measures are taken to limit transient voltages to an appropriately low level. Pollution Degree 2 refers to an operating environment where normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation must be expected.

3.5 Performance Checks

The device has been inspected for mechanical and electrical performance before shipment from the factory. It is free of physical defects and in perfect electrical order. Check the instrument for possible damage in transit and perform the electrical procedures outlined in the section entitled Unpacking and Initial Inspection.

3.6 Power Requirements

The Proteus device operates in a PXIe chassis. DC voltages are supplied to the instrument from the PXIe connector. The instrument requires 3.3 V and 12 V DC voltages. Ensure the PXIe bus is capable of delivering required voltages and has sufficient current to drive the generator. For current consumption refer to Table 12.1 .

Caution
Disconnect power to the PXIe chassis before installing or removing the device.

3.7 Grounding Requirements

To conform to the applicable safety and EMC requirements, ensure that the Proteus device panel and the PXIe chassis are “earth” grounded.

Caution
The outer shells of the front panel terminals are connected to the instrument’s chassis and therefore to the safety ground.

Do not attempt to float the OUTPUT from ground as it may damage the device and other equipment connected to the I/O connectors.

3.8 Calibration

The recommended calibration interval is one year. Calibration should be performed by qualified personnel only.

3.9 Abnormal Conditions

Operate the device only as intended by the manufacturer. If you suspect the device has been impaired, remove it from the PXIe chassis and secure against any unintended operation. The device protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

Warning

Any use of the device in a manner not specified by the manufacturer may impair the protection provided by the instrument

3.10 Long Term Storage or Repackaging for Shipment

If the instrument is to be stored for a long period of time or shipped immediately, proceed as directed below. If you have any questions, contact your local Tabor Electronics representative or the Tabor Electronics Customer Service Department.

1. Repack the instrument using the wrappings, packing material and accessories originally shipped with the unit. If the original container is not available, purchase replacement materials.
2. Be sure the carton is well sealed with strong tape or metal straps.
3. Mark the carton with the model and serial number. If it is to be shipped, show sending and return address on two sides of the box.

Note

If the instrument is to be shipped to Tabor Electronics for calibration or repair, attach a tag to the instrument identifying the owner. Note the problem, symptoms, and service or repair desired. Record the model and serial number of the instrument. Show the returned material authorization (RMA) order number as well as the date and method of shipment. Always obtain a RMA number from the factory before shipping the instrument to Tabor Electronics.

3.11 Preparation for Use

Preparation for use include removing the instrument from the bag, installing the device inside the PXIe chassis, and installing instrument drivers on the control computer. Tabor offers a dedicated software, Wave Design Studio, to manage the device.

3.11.1 Removing the Instrument from the Bag

The Proteus device is supplied in an antistatic bag. Check the seal on the bag to make sure the bag was not opened in a static-unsafe environment. Place the enveloped card on static free surface and hook yourself up with a grounding strap. Only then break the seal and remove the card from the envelope. Hold the card at the metal panel end. Refrain from touching the instrument with your finger at all times.

3.11.2 Installation

To install the Proteus Module in a PXIe chassis, follow the steps below:

1. Power off and unplug the PXI Express chassis.
2. Identify two (or more depending on the options) available and supported PXI Express slots.
3. Touch any metal part of the chassis to discharge static electricity.
4. Place card edges in the dedicated rails at the top and bottom of the chassis and carefully slide the module to the rear of the chassis.
5. When you begin to feel resistance pull up the injector/ejector handle to latch the module.

6. Make sure the metal panel makes contact with the metal edge of the PXIe chassis. Use a suitable screwdriver to tighten the retaining screw to secure the module.

Warning
Once the device is installed in the chassis cover all remaining open slots to ensure proper airflow. Using the device without proper airflow will result in damage to the instrument. It is also recommended to use the highest fan setting available on the chassis to ensure proper cooling of the Proteus device.

3.11.3 Installing Instrument Drivers

The programs, drivers and the user manuals can be downloaded from the Tabor Electronics website at http://www.taborelec.com/downloads. Follow the instructions below to install all the necessary drivers and DLLs on your PC to communicate and control you Proteus device.
The following installation instructions assume that the PXI Express chassis is properly installed and recognized by the controlling PC.

Note
Check the Tabor Electronics website for the most recent software, driver, firmware and documentation updates. www.taborelec.com/downloads.

3.12 Multi Instrument Synchronization

There are applications that require more than the 2 or 4 channels that a single Proteus module can offer. This is where the scalability of the Proteus PXI Express platform can be utilized. Multiple modules can be synchronized within a single PXI Express chassis to create a multi-channel system. The procedure is described in the following paragraphs.

3.12.1 Master Slave Operation

When synchronizing multiple modules, one is designated as the master and the rest as slaves. The master module provides the system clocks and necessary triggers to synchronize and align all of the modules.
The master module must be placed at the left most or lowest numbered available slot in the chassis. Once the master module is inserted, the next slave module must be inserted in the next available adjacent slot and so on until all modules have been placed.

Important
All Proteus modules must be adjacent to one another. There can be no empty slot nor any third-party instruments between Proteus modules.

3.12.2 Connecting the Instruments

Once all the modules have been inserted into the chassis one next to the other, they now need to be cross connected with the designated SMP to SMP synchronization cable. Locate the REF OUT connector of the master instrument (left most module) and attach one end of the cable. Next, connect the other end of the cable to the REF IN connector of the adjacent slave 1 module. Continue

daisy chaining from slave 1 REF OUT to slave 2 REF IN and so on until all modules have been connected.

3.12.3 Operating Synchronized Instruments

When operating two or more synchronized instruments, there are some important limitations to be familiar with in order to achieve optimal performance.

1. Instruments and cables must be placed and connected as described in previous paragraphs.
2. Synchronization mode must be activated either from Wave Design Studio or by SCPI command.
3. Synchronization and channels alignment is automatic.
4. Manual alignment can be performed to improve the skew between channels.
5. Sample clock change is implemented in the master unit alone. Any SCLK change command to one of the slave units will automatically result in the unit exiting from the synchronization mode.
6. Other than SCLK change, each instrument can be independently programmed with a unique set of waveforms, segment table, task table, amplitude, offset and markers.

4 Understanding the Instrument

4.1 Introduction

This section provides a description of the features and functions available in the Proteus module series of arbitrary waveform generators/transceivers.

4.2 General Description

The Proteus module series is a dual- or quad-channel arbitrary waveform generator and transceiver. It is designed to offer outstanding performance with new and advanced capabilities and all this in a compact, modular and easily scalable PXIe platform. Incorporating the most advanced and cutting-edge technology ensures that the Proteus series, is and will be for many years to come, the ideal signal source for many applications.
The module platform offers five different models depending on the SCLK speed and number of channels. The model numbering scheme for the Proteus series, except the P948xM, is shown in the figure below:

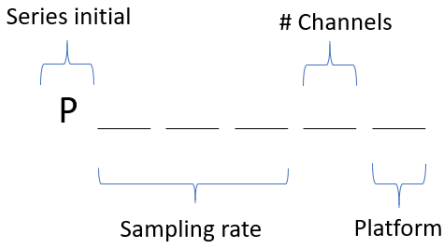

Figure 4.1 Proteus Model Numbering

Example
Model P2582M is a Proteus series model, with a 25 x 10^8 samples per second (2.5 GS/s) sampling rate and 2 output channels based on the Module platform.

The following table summarizes the available Proteus modules.

Table 4.1 Proteus Models vs. GS/s

Sample Rate / Channel Count	1.25 GS/s	2.5 GS/s	9 GS/s
Dual Channel	P1282M	P2582M	P9082M, P9482M
Quad Channel	P1284M	P2584M	P9484M

4.3 System Overview

The block diagram below depicts the core of the system without the options.
The Proteus system is an AWG (Arbitrary Waveform Generators) module, occupying 2 PXIe (PCI Express eXtension for Instrumentation) slots. The main board (Part 1) comes with one DAC (Digital to Analog Converter) and a mezzanine card (Part 2) provides an additional DAC.

There is a DDR4 module for each DAC containing all the wave data, markers data, as well as the task, scenario and segment tables.
System timing and data is controlled through a single FPGA and the communication interface to an external PC is done through 8 lanes of PCIe GEN3.
Various HW options can be added to the AWG module, such as a digitizer, 8 extra digital markers and fast segment dynamic jump. Each of these options adds an additional PCB board that occupies an additional PXI slot.

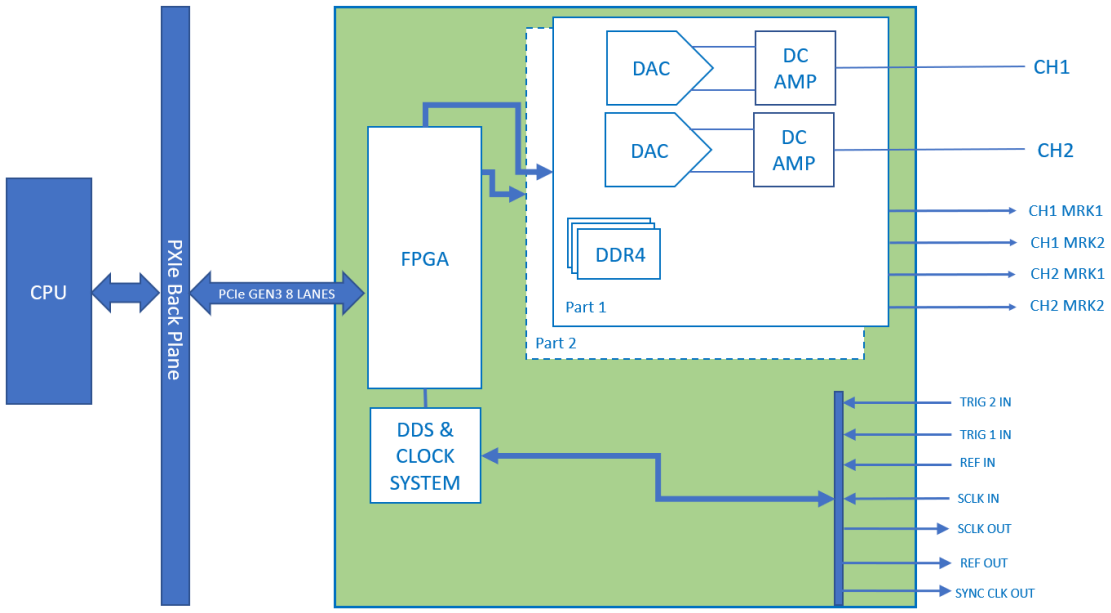

Figure 4.2 Proteus Block Diagram

4.4 Modes of Operation

There are four modes that can be used in order to generate a signal with the Proteus AWG. Direct mode, NCO mode, IQ mode and Streaming mode. An explanation on each of the modes follows.

4.4.1 Direct Mode

In the direct mode the signal being generated is coming from the onboard arbitrary waveform memory. Each part of the unit has a DDR4 module where the arbitrary waveforms are stored. When generating in the direct mode the data stored in the DDR4 is transmitted to the DAC and then to the channel output. When there are 2 channels per part the channels share the same waveform memory. The channels can read from the same segment simultaneously.

Table 4.2 Waveform Sampling Rate Range vs. DAC Sampling Rate as a Function of the Interpolation Factor

Interpolation Factor	Waveform Sampling Rate Range	DAC Sampling Rate
x1 (no interpolation)	SCLK	1e9 - 2.5e9
x2	0.5e9 - 2.5e9	1e9 - 5e9
x4	0.25e9 - 2.25e9	1e9 - 9e9

Notes
The maximum DAC sampling rate depends on the model's sampling rate.

The NCO mode utilizes the integrated Numerically Controlled Oscillator (NCO) to generate sine waveforms. In this mode the arbitrary waveform memory is not used. The frequency generated can be set from DC to the SCLK setting. Each channel has an independent NCO that can generate a different frequency.

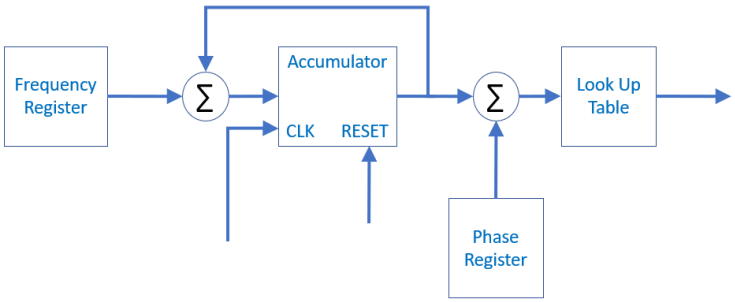

Figure 4.3 NCO Block Diagram

4.4.2 DUC Mode

The Proteus AWG generation capabilities include a wide band digital up-converter, or a wide-DUC (Digital Up-Converter). When using the DUC mode, the IQ complex waveform is stored in the waveform memory and is mixed with the NCO to generate an IQ modulated waveform where the numerical carrier is generated by an NCO.

4.4.3 Streaming Mode

When generating arbitrary waveforms, the amount of data that can be generated is limited by the amount of onboard waveform memory that is available. In addition, it requires having the data prepared in advance and loaded to the waveform memory before generation. The streaming mode of the Proteus AWG enables the user to "by-pass" the on-board waveform memory and continuously generate signals by streaming the waveform straight from the controlling PC, whether from a large file or a real time generation of the data. When using the streaming mode, the sampling rate of the data is limited by the system data transfer rate. The overall sample rate cannot exceed the data transfer rate.

4.5 Channel Outputs

The Proteus AWG can be configured as two or four output channels. The different configurations possible are explained in the 4.3 System Overview. In all configurations the channels are always synchronized and share the same sample clock. Each channel has its own output stage and therefore amplitude and offset are independent and can be set per channel.
There are two types of output configuration options:

- DC Output (standard): This is a differential DC-coupled output stage with variable amplitude control, with up to 1.3 Vpp amplitude and 0.5 V offset in a ±0.75 V window. Bandwidth is limited to work in the first Nyquist zone at maximum sample rate. To use this output in single ended mode, just use the '+' output and attach a high-quality 50 ohm terminator in the '-' output.
- Direct Output (optional): This is an AC-coupled output, with up to 550 mVpp amplitude, optimized for high bandwidth and dynamic range and excellent linearity. Although it is basically designed to be used as a single-ended output (keeping the unused output properly terminated), both '+' and '-' outputs can be used as two opposite-phase outputs if they are connected to impedance-matched loads. Usable BW covers the second Nyquist zone for all the Proteus models even at the maximum sampling rate.

Note
The P948xM comes with DO as default.

4.6 Channel Dependency

As explained in 4.3 System Overview the AWG module consists of a maximum of two DACs with up to two channels per DAC. There are certain dependencies between the channels that need to be taken into consideration when using the instrument.

4.6.1 Inter-Part Channel

The inter-part dependencies relate to dependencies between channels on different DACs.

4.6.2 Dependencies

Clock System

The clock system is common to all channels, so they are always synchronized and share the same sampling rate.

Trigger Source Level

The trigger source level of each trigger input is common to all channels.

4.6.3 Intra-Part Channel Dependencies

The Intra-part dependencies relate to two channels in the same part. Channels in the same part have the same dependencies as channels in different parts with the addition of the segment table.

Segment Table

Each part has a single segment table that is shared between the two channels. However, each channel can access the segment table independently. This means that the channels can simultaneously generate the same segment from the segment table e.g. both channels generate segment 1. This results in efficient memory usage as there is no need to download the same waveform twice. Alternatively, each channel can generate a different segment from the segment table e.g. channel 1 generates segment 10 and channel 2 generates segment 3. Refer to 5.4 Arbitrary Waveform Segments.

4.7 Triggers

While the Proteus system offers versatile waveform creation capabilities these would not be very effective without the ability to tightly control when and how the waveforms start and stop. For this purpose, the Proteus system offers an extremely flexible and sophisticated triggering system that control the start and stop of the waveforms.
The Proteus AWG responds to various trigger sources such as: external trigger signal from the TRIG1 And TRIG2 inputs, Internal trigger generator with programmable trigger period, and BUS trigger for triggering via the controlling PC using software commands.
The trigger source level for TRIG 1 and TRIG 2 inputs is programmed per trigger source and is common to all channels. All other trigger source attributes are independent and can be different for each channel. This means that user can set different trigger parameters for each channel on the same trigger input. In addition, trigger signals are used to both enable and abort waveform or task generation.

4.8 Function Mode

As mentioned in 4.3 System Overview each part of the Proteus AWG has a DDR4 module that contains the arbitrary waveform memory of that part. The waveform memory is where the waveforms that are to be generated are stored. The duration of the generated waveform is limited by the size of the waveform memory.
One can use the entire memory for a single waveform or split the length to smaller segments. In this case, many waveforms can be stored in the same memory and replayed, one at a time, when recalled to the output.
There are two function modes, Arbitrary mode and Task mode, that enable generating the waveforms stored in the memory.

4.8.1 Arbitrary Mode

In arbitrary mode the waveforms that are stored in the memory can be generated one at a time by selecting the segment to be generated. This mode is used when there is no prior knowledge to the order in which the segments should be generated. The selection can be done either by a software command or by external signal if the DJ option is installed.
For a more detailed explanation on the Arbitrary mode refer to 5 Arbitrary Mode.

4.8.2 Task Mode

The other option of playing out the segments is using the Task mode. Task mode enables generating sequences of segments in a predefined order. The user creates a Task table where each task defines numerous parameters such as the segment to generate, loop counter values, condition signals, advancement parameters, and the next task once the current task is done.
One Task table with up to 64K tasks can be defined per channel. In addition to the Task table the user can define a Scenario table. Each line in the Scenario table holds a pointer to a task. The default scenario table contains a single line which points to the first task of the task table. There can be up to 1K lines in the Scenario table.
The figure below describes the workflow of the Task mode. The first task in each sequence of tasks is the reference starting point. Note, a single task can be a sequence. The sequence of tasks is performed until an END state is reached. After this state the next line in the Scenario table is executed, this is repeated until all lines in the scenario table are executed.

Note
Currently, the Scenario table is limited to a single line.

For a more detailed explanation on the Task mode please refer to 6 Task Mode.

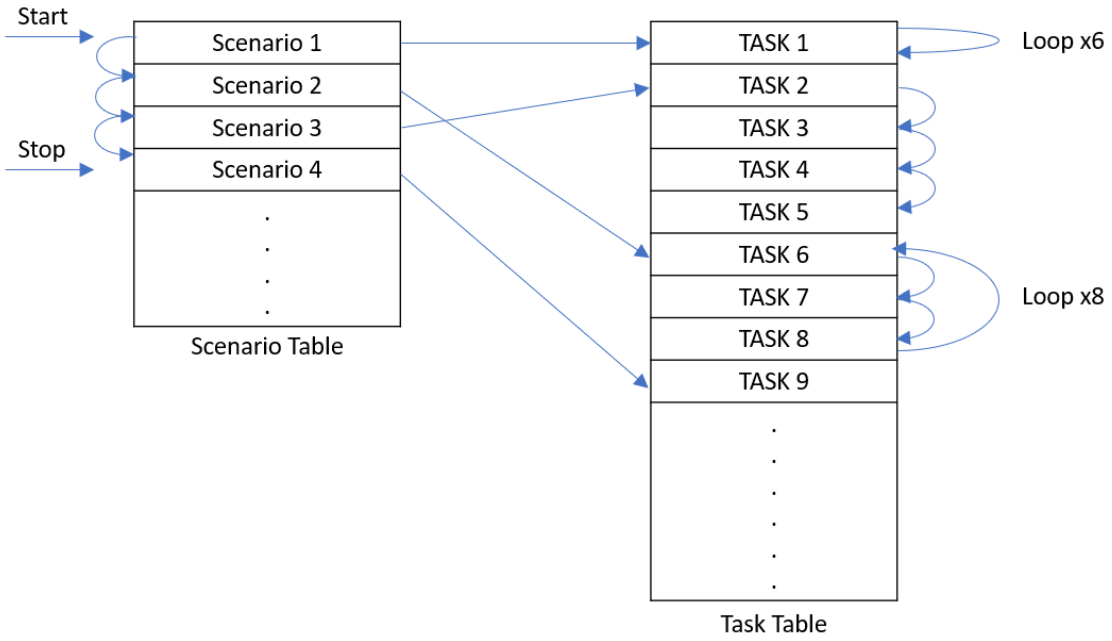

Figure 4.4 Task Mode

4.9 Markers

The Proteus AWG offers additional digital output signals called markers that are synchronized to the analog channel outputs. These can be used as clock signals or control signal for peripheral equipment. The markers data is separate from the waveform data and does not reduce the number of DAC bits available. The markers data is defined per segment and must therefore be identical to the segment length.
The number of markers varies depending on the model, as is shown in Table 2.1 Ordering Information. The number of markers are divided evenly among the channels, e.g., for the 2 channel 4 marker models each channel can have two markers M1, M2.

4.10 Dynamic Segment Control

The Dynamic Jump option (DJ) integrates a 20-pin MDR connector in an additional PXI slot. The 20-pin connector has 2 bits for channel select, 1 bit for valid and 10 bits for data. Hence it is possible to select one of 1024 waveform segments to be generated on any of the channels. Having the dynamic control feature, in effect, can serve as replacement of the task table where the real-time application can decide when and for how long a waveform will be generated. Refer to 13 Appendix A. MDR Interface for a pin description.

4.11 Transceiver

For many of today's applications an advanced arbitrary waveform generator is just a part of the required solution. The waveforms that need to be generated vary depending on input signals from the environment. This type of conditional waveform generation requires not only generating signals but also capturing signals. For this reason, the Proteus series offers an option to transform the arbitrary waveform generator to an arbitrary waveform transceiver or AWT. The Proteus AWT integrates both a DAC and ADC in one system, controlled by a single FPGA for optimal synchronization and minimum latency.
The AWT option, offers an ADC with up to 9 GHz of analog bandwidth and a sampling rate of up to 5.4GS/s in single channel mode or up to 2.7GS/s in dual channel mode. The data captured by the ADC can either be streamed to the PC or stored on the internal waveform memory. When stored in the waveform memory the data can then be transferred to the PC for analysis or can be processed on the on-board FPGA for conditional waveform generation. For more details please refer to the Digitizer section of this manual.

4.12 Streaming

One of the primary concerns in any application that requires an AWG is the duration of the signal or scenario that needs to be generated. Traditionally the playtime duration is determined by the available waveform memory, the sampling rate and the sequencing capabilities of the AWG. In addition, the entire waveform data must be downloaded to the AWG before waveform generation can begin.
The Proteus AWG offers up to 16GS of waveform memory and extremely powerful task mode that is sufficient for most application. However, e.g., radar applications require even longer playtimes. In addition, there are applications like quantum communication where the waveform data cannot be downloaded to the AWG prior to generation and has to be continuously generated.
For applications such as these, the Proteus series instruments offers the capability to continuously transfer waveform data from the controlling PC to the device.
There are two types of methods to transfer the data depending on the data type. Data that has already been created and is stored in a large file and data that is being continuously generated by another process. To distinguish between the two, the latter is referred to as dynamic streaming and the former as file streaming.
When streaming data, the controlling PC must be able to deliver the data faster than it is being generated by the instrument. This means that the hardware, software and interface used are critical in order to achieve maximum throughput.

> **Note**
> The Proteus PXIe modules communicate through a PCIe GEN3 8 lanes, with a throughput of 7.88 GB/s. Considering the encoding scheme overhead (20%) the maximum throughput that can be achieved is ~6.3 GB/s.

Regardless of the streaming type, to achieve optimal data throughput the waveform data should be transferred to the controlling PC RAM. This is to optimize the transfer speed as reading from the RAM is faster than from the PC hard drive.
The data management and synchronization is done using a dedicated API that is provided to the user and runs on the controlling PC. In dynamic streaming mode, the API will provide a pointer to a location in the RAM where the waveform data should be written. When using file streaming the file

path should be provided to the API and the API will manage the file transfer. For more details concerning streaming refer to 4.12 Streaming.

Important
In streaming mode marker outputs are disabled to maximize throughput.

5 Arbitrary Mode

5.1 Introduction

The Proteus Arbitrary Mode is the most direct way to generate a waveform. Waveforms downloaded to segments in the generator's waveform memory can be played back at any sampling rate within the limits of the specific unit. The Proteus family of AWGs implements the "true-arb" architecture. The "True-Arb" architecture is the most flexible and accurate way to generate waveforms numerically. In this architecture, sampling rate is variable within a range and samples are read from the waveform memory in a purely sequential way. In the Proteus platform those samples can be organized in different ways depending on the waveform generation mode being used. Samples are processed in a variety of manners depending on the generation mode before being fed to the DAC. Depending on the model, Proteus modules can incorporate two or four channels with sample rates up to 1.25GS/s, 2.5 GS/s or 9 GS/s. Waveforms generated by each channel can be defined independently although all of them share the same final sampling rate.

5.2 Waveform Memory

The Proteus AWG stores waveforms in a DDR4 memory, see figure below. This memory also keeps other information such as marker states (see 7 Markers) and task and scenario tables (see 6 Task Mode). Samples are read in groups from the DDR so the overall transfer speed, measured is samples per second, is the same than the sampling frequency applied to the DAC, or a submultiple of it when interpolation is active. The maximum size of the DDR memory depends on the model. The P9082M incorporates up to 16G samples of memory per part, all other models offer up to 8G samples per part. Although each bank of DDR4 waveform memory is physically associated to some specific part, the waveform memory can be freely accessed by the different channels (in the case of 2 channels per part) i.e. the two channels can read the same memory segment simultaneously or each channel can read a different segment.

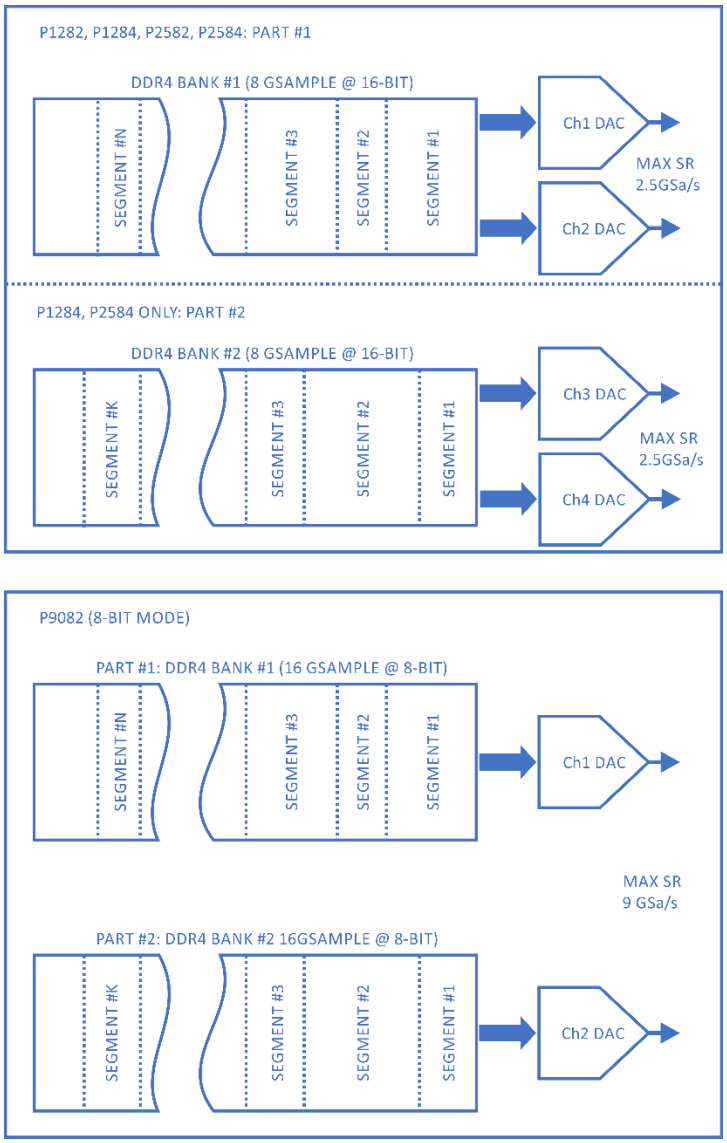

Figure 5.1 Waveform Memory

The internal organization of the waveform memory is based in grouping multiple samples in a 72-bit wide basic word (see below figure). This word carries either 4x16-bit samples or 8x8-bit samples (9GHz model). The additional 8 bits are used to carry two marker states (0/1) for the markers (up to 4 markers per channel) associated to the analog output channel. Marker behavior and set-up is described in section 7 Markers. Eight (8) 72-bit sample/marker groups are read in parallel from the DDR, so 32 16-bit samples or 64 8-bit samples are read simultaneously. The length (in samples) for all waveforms stored in the waveform memory must be a multiple of this number, known as waveform granularity. Optionally, waveform granularity can be reduced by half to 16 or 32 samples respectively. Lower granularity values provide more flexibility and accuracy when defining waveforms. Waveforms stored in the DDR must have a minimum length as well to be use for generation. For the 16-bit Proteus models, minimum length is 1024 samples while for the 8-bit models, minimum length is 2048 samples. Waveforms are stored in waveform segments within the waveform memory. For details, see section 5.4 Arbitrary Waveform Segments.

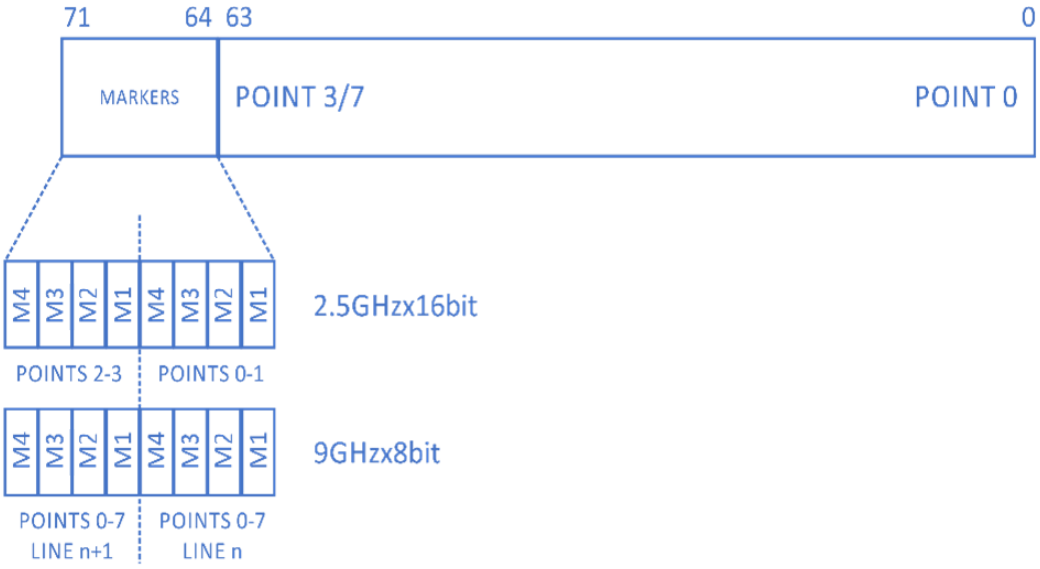

Figure 5.2 Waveform Memory Organization

5.3 Channel Dependency

The different channels in each Proteus module or group share the waveform memory and sampling clock. Other than that, they operate in a basically independent manner. Segments, task and scenario tables are independently defined for each channel so there is no restrictions regarding segment length or sequencing alignment between channels unless this is required by the test being carried out.

5.4 Arbitrary Waveform Segments

Waveform memory can be shared by multiple waveforms assigned to different segments. Segments are typically sections of the DDR4 memory holding a unique waveform. As any waveform, they must match the general requirements for minimum waveform length and granularity (see section 5.2 Waveform Memory). Segments may be used to store multiple waveforms in the waveform memory so they can be selected for generation at any moment without having to download the waveform to the Proteus unit every time it is needed. They can also be used in sequences to synthesize complex waveforms in a more efficient manner (see 6 Task Mode for details). Finally, up to 1024 segments can be selected in real-time through a front panel connector in the optional DJ1/2 Dynamic Jump mode.

The characteristics of each segment is stored in a table associated to each channel called the Segment Table. This table can be defined and maintained though SCPI commands, IVI driver calls or through the WDS software. Segments can be created or deleted by adding or deleting entries into the segment table. These are the basic characteristics of regular segments:

- The maximum number of entries in the segment table for each channel is 64K (64 x 1024).
- There is no limit for the size of a segment other than the available free waveform memory.
- Segments are identified by a unique integer number (1-64K).

- Segments characteristics (segment # and size) must be defined before downloading waveforms to them.
- The whole waveform (or a section of it) for any segment can be update at any moment, even if the generator is outputting that particular segment, without interrupting seamless arbitrary waveform generation.
- One or more entries in the segment table can be deleted freeing the associated waveform memory. This physical memory will eventually be reassigned when some new segment with the same or shorter length is defined.

5.5 Types

Regular segments stored in the DDR4 memory are convenient for most situations. When used in regular sequences, the next segment is read immediately after the end of the current segment iteration. In some event-generated jumps, this means that the time between the event and the actual instant the next waveform starts to be generated may be long and variable as it may depend on the relative timing of the event respect to that of the current segment. Even when setting up "immediate" jumping, time may be long and variable as the DDR4 memory takes time to be reconfigured for the next segment, and samples are transferred in chunks of up to 128 samples. In order to handle this issue, the Proteus platform allows users to store all or part of time-critical segments in a smaller size SRAM. Doing so, switching to the next waveform can be done independently of the DDR4 waveform memory constraints and enjoy much faster and more predictable jumps resulting in a much better trigger jitter performance.
Segments can be classified in three types in the Proteus platform:

- Regular Segments: These are implemented in the large DDR4 memory.
- Fast Short Segments: These segments are fully stored in the internal fast SRAM. Minimum size for short segments is 224 samples for the 9 GS/s units and 64 samples for all others.
- Fast Segments: Only the first samples are stored in the internal SRAM while the rest of the waveform is stored in the big DDR4 memory. When switching to a new fast segment, the first set of samples is read from the SRAM and they start to be fed to the DAC while regular DDR4 memory is set up for the new segment. Minimum size for short segments is 224 samples for the 9 GS/s units and 64 samples for all others.

The maximum number of fast and/or short segments that can be defined for each channel is 128. The maximum length such a segment stored in the SRAM is 8K samples (8x 1024).

5.6 Writing

Segments in the waveform memory can be loaded with waveform data through the appropriate sequence of SCPI commands and data formats. Waveforms can be downloaded in one single transfer process or divided into multiple transfers with arbitrary length sections. In fact, for extremely long waveforms, waveforms cannot be downloaded with a single transfer as the binary data block format does not support transferring blocks of data larger than 999,999,999 bytes (almost 1GByte). The reason for this is the format of the IEEE Std 488.2 binary data block format used along with the :TRACe:DATA command:

:TRACe:DATA #41280<binary_block>

As shown, above, the number of bytes to be transferred is defined by the integer number in ASCII characters before the binary data, and the size of the very same number depends of the previous #N sequence, where N is the single digit number in ASCII format with the digits that must be read in

ASCII format. Therefore, the maximum number of bytes in that transfer can only be expressed with a 9-digit integer. In order to handle waveforms with arbitrary length, waveforms can be split in different sections with supported lengths and be sent in a sequence. As waveform data can be overwritten (or edited) at any time, even while the very same data is being sent to the DAC for conversion, it is also useful being able to transfer just portions of the waveform when just a portion of the waveform must be updated. Finally, splitting the waveform in multiple sections can be used to update the GUI of the control SW during long transfers. Although transfer rates supported by the PCIe bus allow to download 1 G sample in under one second, sometimes data may be downloaded as it is calculated and calculation time may be quite long so the application may be stuck during this process unless data calculation and transfer is interrupted from time to time. This is a complete sequence of commands/actions required to successfully download a waveform to a segment in a given Proteus unit.

1. Select the channel for download (command :INST:CHAN:SEL{1|2|3|4})
2. Create the segment if not already created (:TRAC:DEF <SEG_NUMBER>,<SEG_LENGTH>)
3. Select the segment for download. Not necessary if next target for waveform data is the last segment created in step #2.
4. Download the section of the waveform. Section size is embedded in the binary block header (:TRAC:DATA[<OFFSET>,]#<HEADER><BINARY_BLOCK>)

1. Go to step #4 until the complete section has been downloaded.

The above sequence reflects the most general case. To make downloads easier in many cases, the pointer for the next sample to be downloaded is set to 0 (first sample in the segment) right after selecting or creating a segment. This pointer is updated after successfully downloading a given number of samples.

5.7 Reading

Waveforms can be read from the internal waveform memory in a very similar manner to the way they are written. The sequence of reading a waveform is the same as step 1 to 4 in writing a waveform, refer to section 5.6 Writing. However, unlike the writing process where the size of the segment is previously defined and the size for each transfer is specified (in bytes) as part of the binary block header, the reading process requires one extra steps in order to define the data to be read:

1. Determine the total size of the segment to be read in case is not already known (command :TRAC:DEF?).

The waveform data received from the Proteus unit is formatted in the same way binary blocks for waveform downloads are:

#Nn..n<binary_block>

5.8 Streaming

AWGs typically generate signals based on waveforms stored in the waveform memory. These waveforms may be used directly or after a series of processing steps (sequencing, interpolation, real-time filtering, digital up-conversion). Although the waveform memory may be very big, it can be insufficient for some applications. In some other cases, waveforms must be calculated in real-time as they are being generated. In order to support such scenarios, the Proteus platform supports real-time streaming from the PCIe backplane (part of the PXIe bus). Proteus provides PCIe Gen3 8-lanes wide. This interface supports an overall raw data rate of around 50 Gbps. This results in a

seamless conversion rate of over 6GS/s for one AWG channel using 8-bit samples. The available BW must be shared among channels in the same or different modules.

6 Task Mode

6.1 Introduction

The Proteus AWG platform supports an advanced waveform generation mode named Task Mode. Within Task Mode, users can define a table for each channel made of up to 65,536 entries. Each entry fully specifies the way a given segment is going to be generated. One segment can be assigned to any number of task entries or not any entry. Tasks can be simple, independent single segment generation schemes, or they may be part of a complex sequence with synchronous or asynchronous, conditional or unconditional jumps to other tasks depending on events defined for each task. Tasks also define what to output during idle periods (before the task enabling event or after the current task has been completed and the generator is waiting for the next jumping event).
Each task points to a single segment and the same segment may be pointed by different tasks. For the P128x, P258x, and P948x models, segments are shared by channel pairs (ch1/ch2 and Ch3/ch4 pairs) so even tasks from different channel can point to the same segment.
Both tables, Task and Scenario, can be defined entry by entry from the WDS (Wave Design Studio) GUI (Graphical User Interface) or through SCPI (Standard Commands for Programmable Instruments) commands. These commands allow for the definition in a readable format of each entry and the corresponding parameters one by one, or they can be handled in a more efficient, fast and compact way by transferring the whole or parts of those tables in binary format to the device.

6.2 Task Table

There is a unique Task table defined for each channel. Each table can hold up to 65,536 entries. There are two types of tasks:

- Single task: Segment, number of loops, enable and disable events, jumping mode and next task (if any) to be generated are defined. This means that single tasks can be member of a complex sequence.
- Sequence task: There are three subtypes of Sequence task: *StartSequence*, *InsideSequence*, and *EndSequence*. Sequence tasks behaves identically to Single tasks, but they can be grouped as an independent entity that can be looped any number of times (or indefinitely). The purpose of this task type is to simplify the creation of complex sequences, where sections of it must be repeated a given number of times. Otherwise, each repetition should be implemented by additional entries in the Task Table (one for each loop), consuming resources in terms of table space, table creation code and download time. The location of tasks associated to a given segment within the task table is not limited. This means that segments part of the same group do not have to be contiguous and that the “single” and “sequence” tasks can be located anywhere in the table.

Sequencing is the most important functionality added by the Task Mode. Sequences can be linear , so one task can be executed after the other as they are listed in the Task Table, or they can be generated in a non-linear way, as the next task to be executed after the completion of the current task is one of the task attributes that can be defined by the user. Jumping from one task to the other can be controlled by events generated by software (i.e. the ***TRG** SCPI command) or different internal or external trigger signals. Jump destination can be deterministic to a single predefined task

or it may be selected among several choices depending on the event generating the jump allowing for conditional branching.
The best way to handle such a complex, flexible and powerful sequencing scheme, is by thinking of it as a state machine where tasks are the states and events control the transition between states. A very institutive way to design and visualize such state machines are state diagrams. An alternative representation of the sequencer functionality is a flow chart. Flow charts are probably the best tool to handle the Task Mode in Proteus as it directly shows the behavior of the sequencer in the time-domain. From now on, flow charts will be used to illustrate and define the Task Table functionality. The following graph shows the type of blocks relevant to this situation.

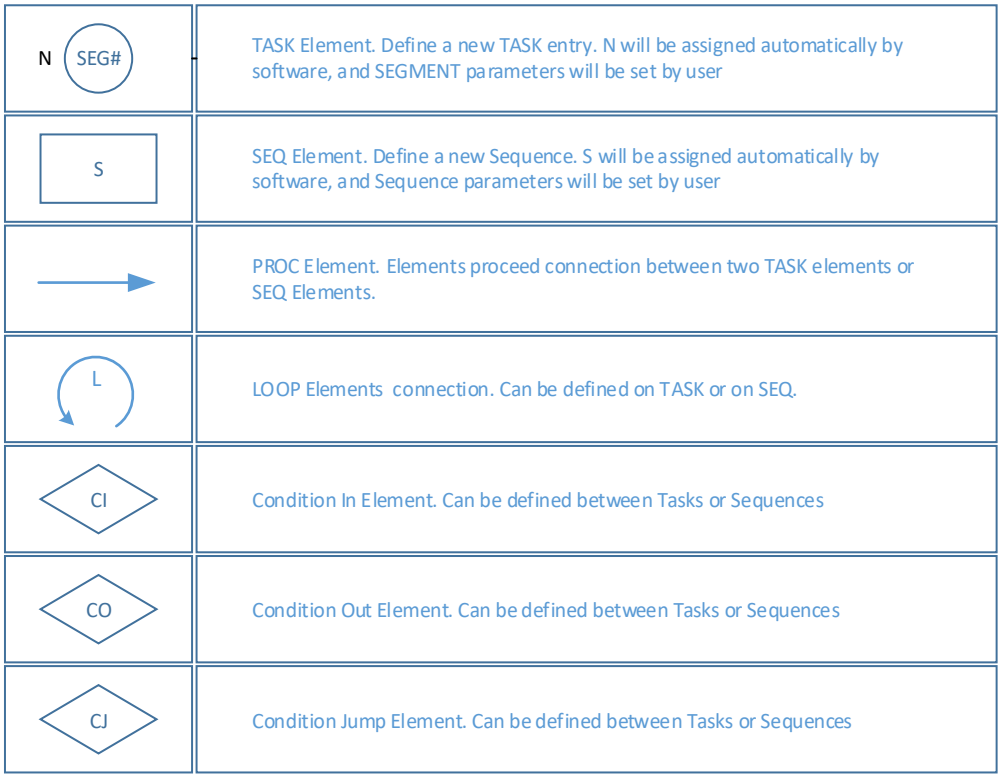

Figure 6.1 Type of Blocks Implemented by the Task Table

Additionally, a given task can also define the behavior of the output channel during the “idle” state, the period before the task itself is enabled by the designated event or after the completion of the current task and before jumping to the next task as set by the *Next task Delay* parameter. The aborting conditions (so the current task is terminated) can also be defined for each task. Finally, the number of repetition loops for the associated segment can be set form 0 (continuous) to 1,048,576. Jump can take place as soon as the Aborting event is received (Immediately) or after the current loop is finished (Eventually).
Figure 6.2 below shows an example of a task table using the blocks shown in Figure 6.1 Type of Blocks Implemented by the Task Table
above. The green numbers indicate the task numbers, the blue numbers in the circle indicates the segment number, CI indicates a Condition In (e.g. Enable signal), CO indicates Condition Out (e.g. Conditional jump).

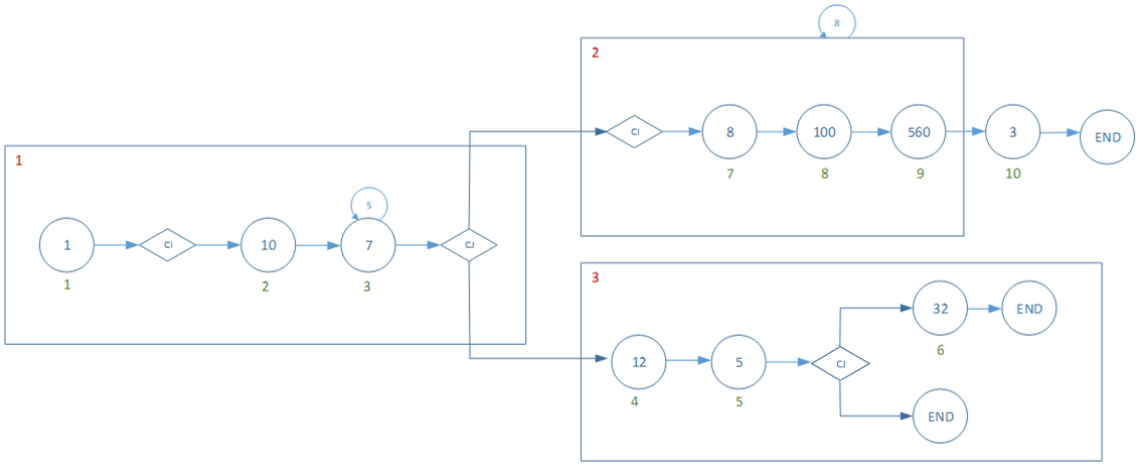

Figure 6.2 Flowchart for an Example Task Table

6.3 Task Table Parameters

Tasks are defined by a series of parameters associated to each task. Although all these parameters are included in the Task Table for each entry, not all of them may be active as there are some interdependencies. Below are the parameters, their possible values and states, and a description of the corresponding functionality. Refer also to WSD, SCENARIO COMPOSER, Task in the WSD User Manual.

- **Task No.**: This is just the number of the entry in the table. It is automatically assigned when a new task is defined. Task can be selected by using this unique number.
- **Task State**: It indicates the type of task for that entry. It allows for the definition of groups of tasks that can be used together as a single entity so looping for it can be defined independently of the member tasks. These are the possible choices:
  - **Single**: An independent task not being part of a group of tasks.
  - **StartSequence**: This type of task defines the beginning of a group of tasks to be used as a group. The loops for the group must be defined for these tasks in the corresponding parameter (“Sequence Loops”).
  - **InsideSequence**: This type of task defines a task within the grouped tasks.
  - **EndSequence**: This sequence defines the final task within the group. After terminating this task, the group will be looped again from the StartSequence task until the defined number of loops have been completed. Once this condition is matched, the next task will be controlled by the jump definition parameters for this task.
- **Task Loops**: This is the number of times for the task to be looped. It can go from 0 (continuous looping) until 1,048,576 times.
- **Sequence Loops**: This is the number of times for the grouped tasks to be looped. It can go from 0 (continuous looping) until 1,048,576 times. This parameter is only active when Task State is set to StartSequence.

- **Seg Number**: This is the segment number pointed by the current task. This will be the segment fed to the DAC for generation. The same segment can be referenced by any number of tasks. Channel 1&2 and 3&4 in the P128X and P258X models share the same segments for each pair so the same segments can be referenced by tasks in Task Tables for each channel.
- **Idle Waveform**: It states the behavior of the output before the effective generation of the waveform segment pointed by the current task takes place, the so called “idle state”. The “idle state” can be active while the sequencer is waiting for the enabling event or when a delay is forced through the Task Delay parameter. These are the possible choices:
  - **DC**: This is just a user-defined fixed voltage specified in DAC levels (0-255 for the P908X and 0-65,535 for the P128X and P258X models).
  - **FirstPoint**: This is a fixed voltage level specified by the value of the first sample in the segment pointed by the current task.
  - **CurrentSeg**: The segment pointed by the current task will be generated during the “idle state”.
- **DC Value**: This is the user-defined fixed voltage specified in DAC levels (0-255 for the P908X and 0-65,535 for the P128X and P258X models) for the Idle Waveform state while in the “DC” mode.

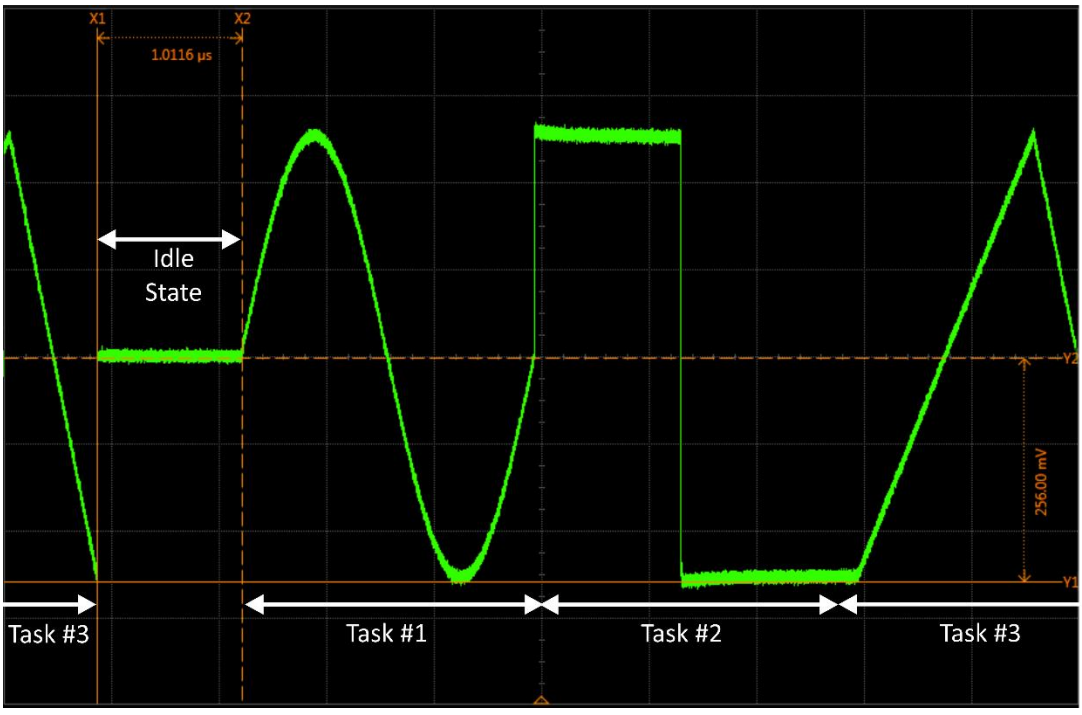

Figure 6.3 DC Level Idle State Associated to Task #1

- **Enabling Signal**: The following sources can be used to initiate the execution of a given task:
  - **None**: The task is initiated immediately (after the time set buy the Task Delay parameter).

- **ExternTrig1**: External Trigger input 1. Trigger 1 settings are set independently.
- **ExternTrig2**: External Trigger input 2. Trigger 2 settings are set independently.
- **InternTrig**: Internal Trigger Source.
- **CPU**: Bus trigger through SCPI commands (*TRG).
- **FeedbackTrig**: Trigger from the digitizer block in the optional AWT module (decision block). The trigger conditions are set independently.
- **HwControl**: Using the optional FS1/2 module.

- **Aborting Signal**:
  - **None**: The task is terminated immediately after the number of loops defined in the Task Loops parameter.
  - **ExternTrig1**: External Trigger input 1. Trigger 1 settings are set independently.
  - **ExternTrig2**: External Trigger input 2. Trigger 2 settings are set independently.
  - **InternTrig**: Internal Trigger Source.
  - **CPU**: Abort signal through SCPI commands (*TRG).
  - **FeedbackTrig**: Trigger from the digitizer block in the optional AWT module (decision block) associated to the digitizer section (AWT models) . The trigger conditions are set independently.
  - **AnyExternTrig**: Any of the external trigger inputs (Trigger 1 and Trigger 2) when activated according to the respective settings set independently.
- **Jump Mode**: Jumping can be synchronous or asynchronous with the generation associated to the task. According to the expected behavior, Jump Mode can be set to one of these two modes:
  - **Eventually**: After detecting a valid trigger signal for jumping, jump is carried out after full play back of the current loop of the associated segment.
  - **Immediately**: This is used in conjunction with an abort signal or conditional jump. Jump is carried out as fast as possible after detection of the jumping conditions. The latency between a valid trigger to a change in the output is determined by the system delay of the unit and varies depending on the sampling clock. However as long as the system settings are constant the latency time is deterministic (not including the trigger jitter).

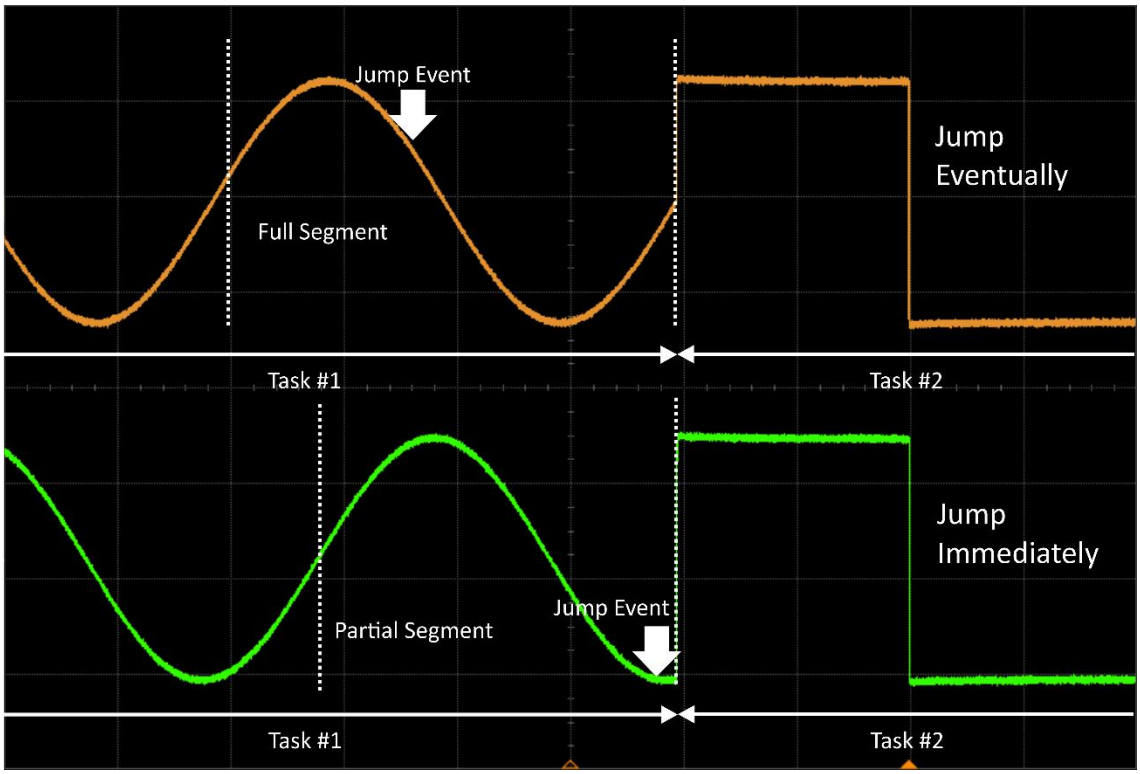

Figure 6.4 Different types of Jumps. Jump Eventually (Top) and Jump Immediately (Bottom)

- **Jump Destination**:
  - **Next1Task**: Next task as designated by the Next task 1 parameter.
  - **FeedbackTrigValue**: Task number set by the Feed-Back Trigger coming from the decision block associated to the digitizer section in the optional AWT.
  - **SwitchNext1Next2**: Next task will be defined by either the Next Task 1 (TRIG1) or the Next Task 2 (TRIG2) parameter depending on the first valid trigger event detected from either the External Trigger 1 or External Trigger 2 sources.
- **Next Task 1**: Task 1 number for the Next1Task and SwitchNext1Next2 jump destination.
- **Next Task 2**: Task 2 number for the SwitchNext1Next2 jump destination.
- **Task Delay**: This is a delay expressed in an integer number of sample periods to effectively start the current task. During this period, the output is in the “idle state”.
- **Loop with Trigger**: When a task has an enable signal and a task loop count larger than 1 this selects whether a trigger outputs all of the task loops or just one loop. For example, a task is looped three times and TRIG1 is the enable signal, when the Loop with Trigger is disabled, a single trigger is required to advance to the next task. When the Loop with trigger is enabled three triggers are required to advance to the next task.
- **Trigger ADC:** The task will generate an internal trigger signal that will trigger any digitizer channel where the trigger sources are assigned to this particular task, which is associated to an specific AWG channel.

6.4 Task Table Limitations

While the task mode offers powerful and flexible sequencing features there are certain limitations that the user must adhere to when programming the task table.

6.4.1 Conditional Jump

When using the conditional jump capability, the destination task must meet the following conditions:

1. The segment must be a Fast Short Segment see 5.5 Types.
2. There cannot be an enable signal, an abort signal, a task delay or a task loop greater than 1.
3. Task state cannot be end of sequence.
4. Jump destination must be Next1Task.

6.4.2 Segment Transitions

When transitioning between segments it is not possible to transition from a Fast-Short Segment to a regular segment. Only Fast Segments can transition to regular segment.

6.4.3 Trigger Signal

When using a trigger signal in task mode in conjunction with jump mode eventually there is a minimum hold off time that must be observed in order for the unit to detect the trigger. The trigger signal must be at least 64 sample clocks after the end of the segment in the 9GS/s units and 16 sample clocks after the end of segments in all the other units.

6.5 Scenario Table

The scenario table implements an upper layer of task execution control. Each entry in the Scenario Table point to a given task and specifies a number of loops (repetitions) for each entry. As tasks pointed by the Scenario table can be sequences, this scheme allows for the definition of “sequence of sequences” kind of scenarios. The last task in the sequence must contain “Next Scenario” as its Jump Destination definition. In this way, control is returned to the Scenario Table so it can repeat the same task, if the number of loops set for this entry is not completed or jump to the next entry. The Scenario Table is defined independently for each channel and can keep up to 1024 entries. When the Scenario Task is not defined, there is a “default scenario” launching task # 1.

7 Markers

7.1 Introduction

The Proteus series of instruments offers programmable digital output signals that are synchronized to the main analog outputs. These signals are referred to as markers. The purpose of these markers is to provide auxiliary outputs, that are fully synchronized with the output waveforms, for control of peripheral equipment or as additional digital data stream. Each channel output can have between 1 – 4 corresponding marker outputs depending on the model and the configuration. The number of markers are divided evenly among the channels, e.g., for the 2 channel 4 marker models each channel can have two markers M1, M2.

7.2 Marker Control

Control of the markers is done by addressing each marker separately. Each marker output can be programmed to have a unique set of data, amplitude, DC offset and time delay. The amplitude and DC offset of each marker can be set using the relevant voltage and offset SCPI commands or in WDS. The markers are aligned so that the skew in time between the analog channels and the markers is kept to a minimum. In addition, it is possible for the user to add delay in time for each marker with respect to the analog channel outputs. The delay can be set in either sample clock periods or in units of time.

7.3 Programming the Markers

When a segment is defined in the segment table it has its corresponding wave data and marker data. Every time a segment is generated the corresponding waveform and markers are generated. There is a defined relationship between waveform data and marker data. There is one byte of markers data per eight bytes of waveform data. The ratio between the number of wave points and marker points depends on the Proteus model.

7.3.1 P9082X Models

For the 9GS/s model there is one markers-point per eight waveform-points, and the sampling rate of the markers is 1/8 the sampling rate of the waveform.
For example, if a segment of 4096 waveform points is defined, then it is necessary to download:

- 4096 bytes of waveform data that hold 4096 waveform points
- 512 bytes of markers data that hold 512 markers-points.
- For every byte of marker data, the routing is as follows:

Table 7.1 Byte of Marker Data 9 GS/S Models Channel 1/2

Bit 0	Marker 1
Bit 1	Marker 2
Bit 2	Marker 3
Bit 3	Marker 4
Bit 4	N/A
Bit 5	N/A
Bit 6	N/A

Bit 7	N/A

Example

Assume that we have defined a segment of 32 waveform points. The waveform data consists of 32 bytes (1 byte per waveform point). Let's download waveform-data that represents one cycle of sinusoid waveform.

Reminder

The 32 points segment is for example purposes. The minimum segment size for 9GS/s model is 256 points.

The markers data consists of 4 bytes (1 byte per marker point for 8 waveform points). Let's download the four markers bytes: 0x01, 0x02, 0x04 and 0x08.
It means that during the first eight ticks of the sampling clock marker 1 is high, during the next eight ticks marker 2 is high and so forth.

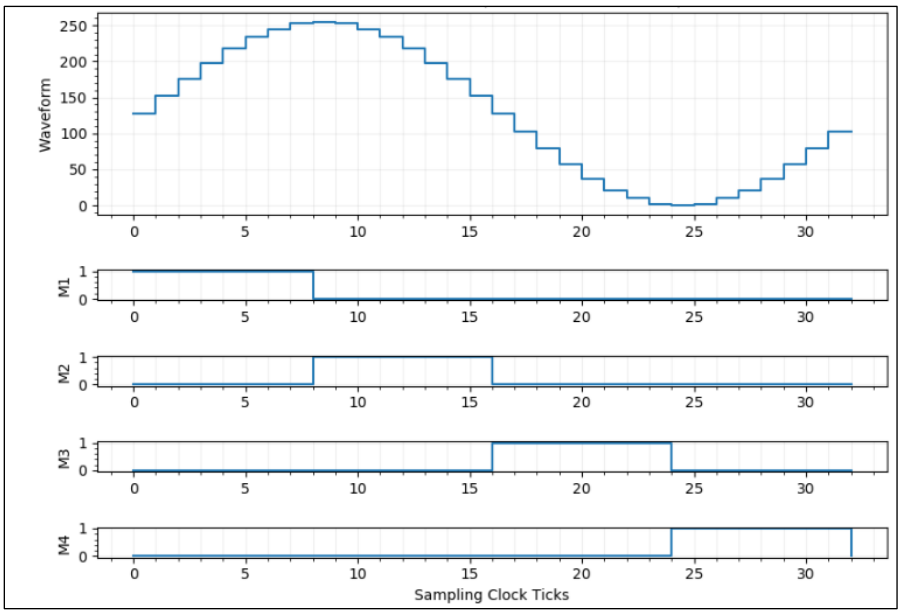

Figure 7.1 9 GS/s Model - 32 Waveform Points and 4 Marker Points

Segment Data

Waveform Data	
Index	Byte (decimal) value
0	128
1	152
2	176
3	198
4	218
5	234
6	245
7	253
8	255
9	253
10	245
11	234
12	218
13	198
14	176
15	152
16	128
17	103
18	79
19	57
20	37
21	21
22	10
23	2
24	0
25	2
26	10
27	21
28	37
29	57
30	79
31	103

Markers Data	
Index	Byte (decimal) value
0	1
1	2
2	4
3	8

Figure 7.2 Segment Data

7.3.2 All other Models

For the 1.25 GS/s and 2.5 GS/s models there is one markers-point per two waveform-points, and the sampling rate of the markers is half the sampling rate of the waveform.
In this case each waveform point occupies 2-bytes, and each byte of marker-data holds two marker-points.
For example, if a segment of 2048 waveform points is defined, then it is necessary to download:

- 4096 bytes of waveform data that hold 2048 waveform points
- 512 bytes of markers data that hold 1024 markers-points.
- For every byte of marker data, the routing is as follows:

Table 7.2 Byte of Marker Data 1.25 GS/S and 2.5 GS/S Models

Bit 0	Marker 1
Bit 1	Marker 2
Bit 2	N/A
Bit 3	N/A
Bit 4	Marker 1
Bit 5	Marker 2
Bit 6	N/A
Bit 7	N/A

Table 7.3 Byte of Marker Data 1.25 GS/S and 2.5 GS/S Models

Bit 0	Marker 1
Bit 1	Marker 2
Bit 2	Marker 3
Bit 3	Marker 4
Bit 4	Marker 1
Bit 5	Marker 2
Bit 6	Marker 3
Bit 7	Marker 4

Example

Assume that we have a P2582M model, and we defined a segment of 8 waveform points. The waveform data consists of 16 bytes (2 bytes per waveform point). Let's download waveform-data that represents one cycle of sinusoid waveform.

Reminder

The 8 points segment is for example purposes. The minimum segment size for 1.25GS/s or 2.5GS/s models is 64 points.

As there are 2 waveform points per marker point, the markers data consists of 4 marker points or 2 bytes (2 marker points per byte). Let's download the two markers bytes: 0x21, 0x84.
It means that during the first two ticks of the sampling clock marker 1 is high, during the next two ticks marker 2 is high and so forth.

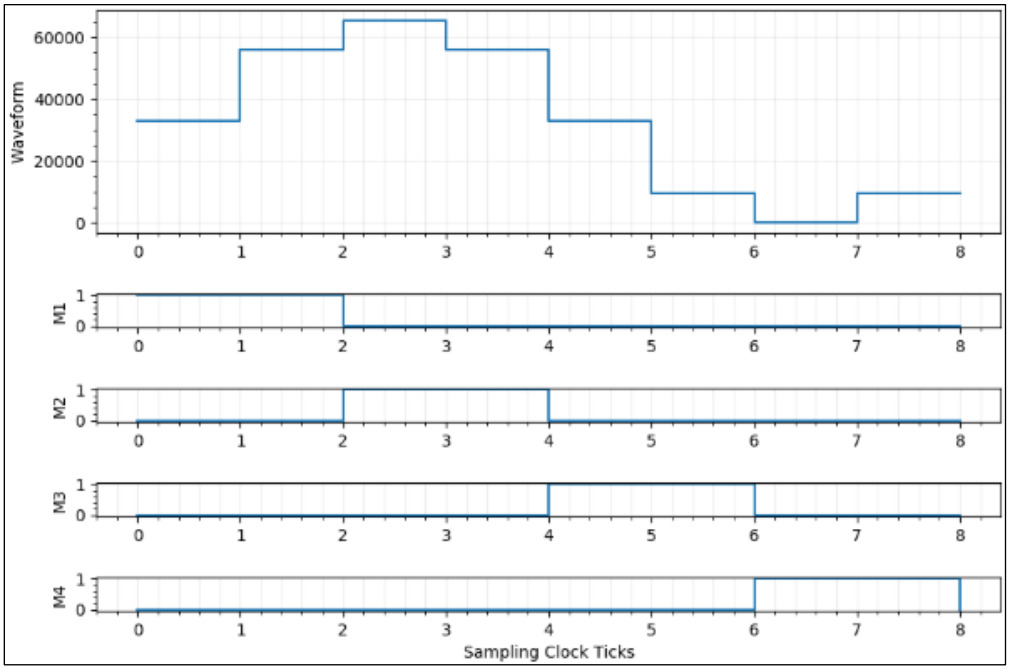

Figure 7.3 P2582M Model 8 Waveform Points and 4 Marker Points

Segment Data

Waveform Data

Index	Word (decimal) value
0	32768
1	55938
2	65535
3	55938
4	32768
5	9597
6	0
7	9597

Markers Data

Index	Byte (decimal) Value
0	33
1	132

Figure 7.4 Segment Data

8 DUC Operation

8.1 Introduction

The Proteus P9482/4M and P2582/4M series (DUC option) incorporate a DUC (Digital Up-Converter) block associated to each output channel.

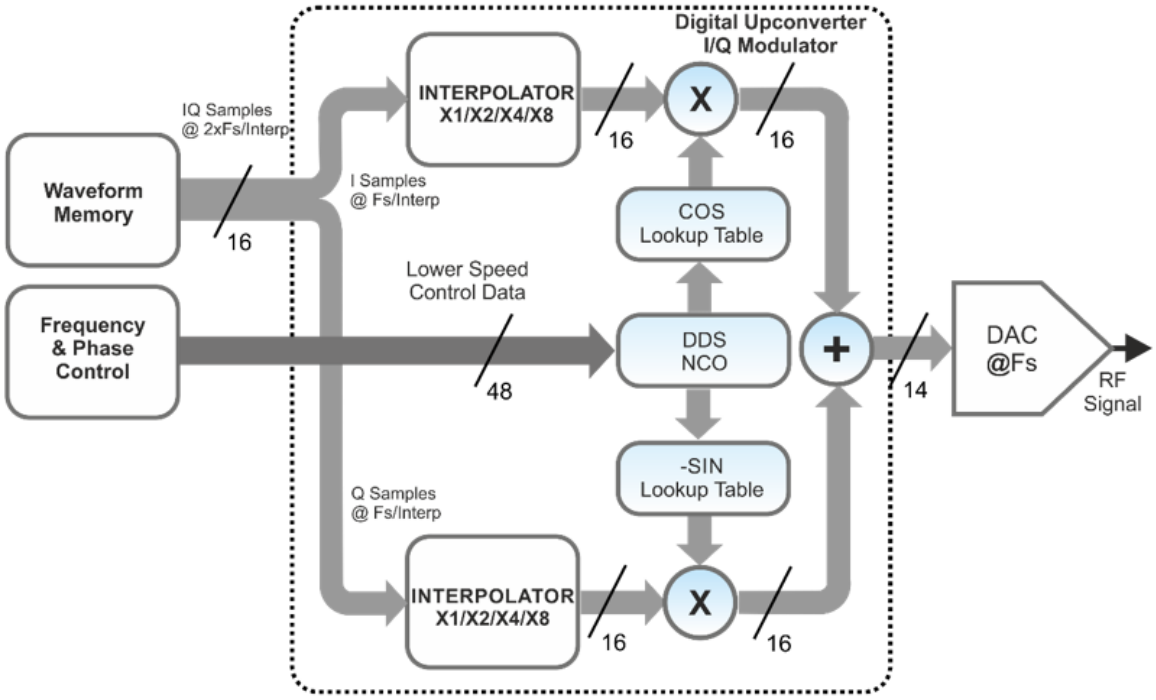

Figure 8.1 IQ Modulator Block Diagram

This block incorporates two independent and parallel up-conversion stages. Up-conversion is implemented through the numerical quadrature modulation of one or two I/Q baseband streams (complex signals) read from the waveform memory. Each quadrature modulator is associated to a quadrature NCO (Numerically Controlled Oscillator) which frequency and phase can be independently controlled and updated without interrupting signal generation. As the bandwidth of the modulating I/Q signals may be significantly lower than the carrier frequency, the baseband signals go through a variable interpolation stage. This means that the ratio between the DAC sampling rate and the one for the I/Q baseband signals can be 2X, 4X, or 8X, resulting in important savings in terms of waveform size and calculation and download time. The right interpolation factor and sampling rate may be selected depending on the modulated signal characteristics including modulation bandwidth and carrier frequency.

Table 8.1 P948X Maximum DAC and I/Q Sample Rate (SR)

Mode	X1	X2	X4	X8
NCO	DAC SR: 9GS/s IQ SR: N/A	DAC SR: 9GS/s IQ SR: N/A	DAC SR: 9GS/s IQ SR: N/A	DAC SR: 9GS/s IQ SR: N/A
ONE	DAC SR: N/A IQ SR: N/A	DAC SR: 2.5GS/s IQ SR: 1.25GS/s	DAC SR: 5GS/s IQ SR: 1.25GS/s	DAC SR: 9GS/s IQ SR: 1.125GHz
TWO	DAC SR: N/A IQ SR: N/A	DAC SR: N/A IQ SR: N/A	DAC SR: 5GS/s IQ SR: 612MS/s	DAC SR: 9GS/s IQ SR: 562MS/s
HALF	DAC SR: 2.5GS/s IQ SR: 2.5GS/s	DAC SR: 5GS/s IQ SR: 2.5GS/s	DAC SR: 9GS/s IQ SR: 2.25GS/s	DAC SR: N/A Mod. BW: N/A

The P948xM and P258xM support a variety of DUC-related operating modes.

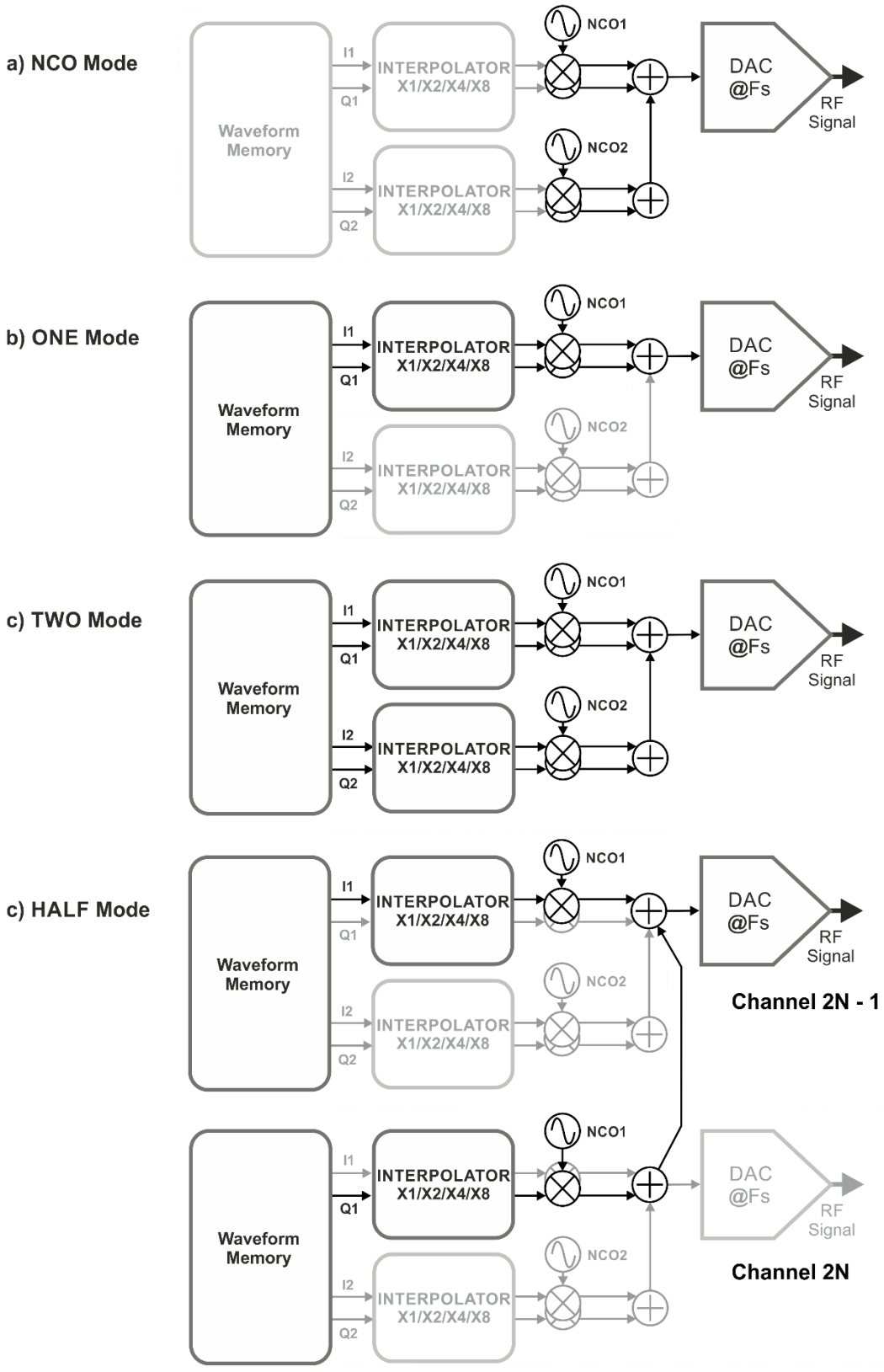

Figure 8.2 DUC Working Modes for Proteus P948X and P258X

- **NCO Mode** – In this mode, no modulating waveform is required. It can be used to generate sinewaves with user-defined parameters including frequency, phase, and amplitude. As there are two independent NCOs, two different frequencies may be generated simultaneously by each channel.
- **ONE Mode** – This mode up-converts a single IQ stream using IQ modulator #1.
- **TWO Mode** – Two different IQ streams are fed to each IQ modulator for the designated channel. Both streams will be interpolated by the same factor so the IQ waveforms must be created with the same sampling rate and they are read as a single entity from the waveform memory.
- **HALF Mode** – The 'half' mode is designed to double the available modulation bandwidth by using the resources of two channels for a single IQ pair. Therefore, the number of effective signals that will be generated in that mode will be half of those created in the previously described modes.

The above modes can be independently set for each channel (or pair of channels for the 'two' mode). Each mode requires the waveform data to be properly calculated, normalized, and formatted before it can be effectively downloaded and played back.

8.2 NCO Mode

The NCOs implemented in the up-conversion blocks use the DDS (Direct Data Synthesis) architecture, refer to Figure 8.2 a). Their frequency can be controlled with high accuracy and resolution independently of the final sampling rate for the DAC or any consideration about the modulating waveforms. Even more, frequency (and phase) can be changed "on the fly" with continuous phase by updating the frequency setting for that NCO. The DDS's phase accumulator points to two lookup tables, each one with a sine and cosine reference waveform. The output of each one of the tables goes to the I and Q multipliers, respectively. In the NCO mode, IQ sample pairs are not fed to the multipliers, so an unmodulated waveform can be generated without any need to define any waveform to be played back.

The NCO's frequency can be set to any value from DC (0 Hz) to the current sampling rate. As a result, the intended carrier frequency can be applied in the first and second Nyquist Zones, see Figure 8.3 3a). In this way, users do not have to calculate the first Nyquist Zone image frequency to obtain the right frequency in the second Nyquist Zone. Additionally, the right phase will be applied to the carrier in the second Nyquist band. Otherwise, the phase for the carrier in the second Nyquist band would that of the complex conjugate complex carrier, see Figure 8.3 3b).

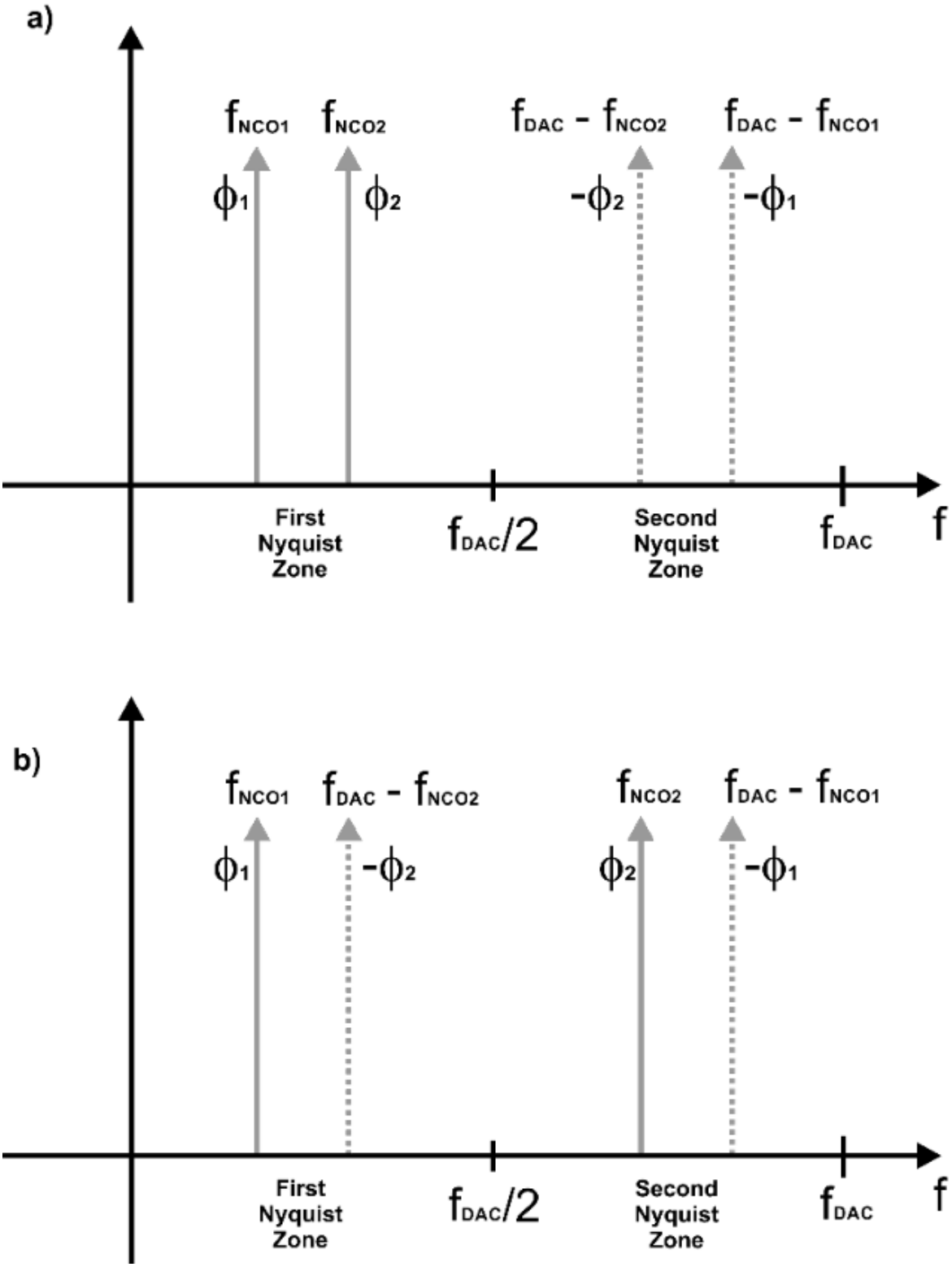

Figure 8.3 Effects of Setting the NCO Frequency within the First (a) and the Second (b) Nyquist Band

However, the unwanted image in the first Nyquist zone will stay and it should be removed, if necessary, through the usage of a BPF (Band Pass Filter) for the carrier in the second Nyquist zone or a “notch” filter for the unwanted carrier in the first Nyquist Zone.
In the NCO mode, both NCOs can be set independently. However, the DAC could be clipped if both NCOs used the full amplitude range for the DAC. The worst-case amplitude for the combined output would be twice the available dynamic range. For this reason, there is a switchable 6 dB attenuation stage at the output of each NCO. Reducing the amplitude of the output to half (-6 dB) makes sure that the combined two carriers will not clip the DAC output, no matter the frequencies being generated.

8.3 ONE Mode

In the ‘ONE’ mode, the primary IQ modulator associated to NCO #1 is used to upconvert a complex baseband signal (made of I and Q components) to the designated band according to the frequency set for the NCO (Figure 8.2 2b). Initial phase can also be set to any desired value. When multiple channels are set to the same frequency, the relative phase between those channels can be defined so any set of signals for applications such as MIMO (Multiple-Input Multiple-Output), Beamforming, or Phase Array (AESA – Active Electronically Scanned Array) Radar can be easily implemented. Unlike Direct DAC mode, in ‘ONE’ mode, the two baseband signals, I and Q, must be stored and transferred together to the waveform memory. I and Q waveforms, once calculated, must be quantized and interleaved to build the combined waveform to be downloaded to the selected segment.

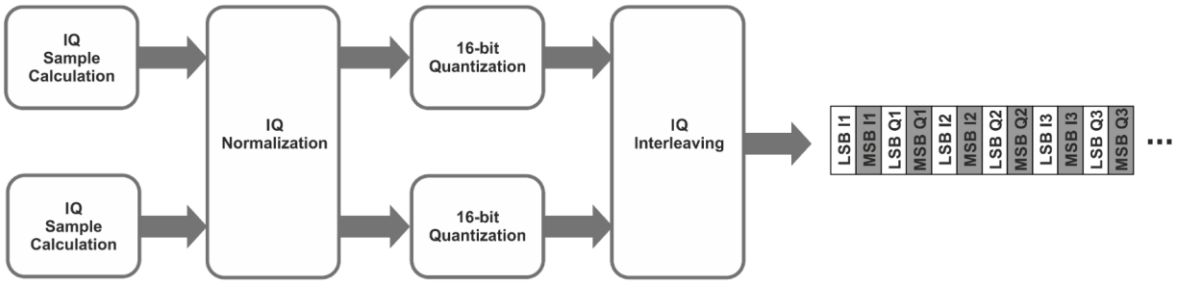

Figure 8.4 I/Q Sample Processing for Download to the Waveform Memory in Proteus Working in the DUC ‘ONE’ Mode

Waveform length granularity conditions still apply to complex interleaved IQ waveforms, so the number of the complex samples before interleaving must be a multiple of half the granularity for the generator. Baseband waveforms must be calculated at the right sampling rate, equal to the DAC’s sample rate divided by the interpolation factor. Interpolation factor can be chosen among the 1X, 2X, 4X, and X4 choices. Not all the interpolation factors are valid for every sample rate as the effective 16-bit sample transfer rate from the waveform memory cannot be higher than 2.5 GS/s for each channel. Effective sample rate from the waveform memory is twice the sample rate for the baseband complex waveform. Table 8.1 shows the maximum DAC sample rate that can be set for a given interpolation factor. The combination of DAC sample rate and interpolation factor must be selected in such a way that the complete spectrum of the modulating signal can be accommodated within the available modulation bandwidth.
As shown in the ‘NCO’ mode, the carrier frequency for the NCO attached to the IQ modulator stage can be set to any frequency between DC and the DAC’s sample rate. The generation of a modulated waveform in the second Nyquist Band requires setting the NCO’s frequency to the right image frequency in the first Nyquist Band. However, modulating this carrier with the intended I/Q waveforms will result in an inverted spectrum in the Second Nyquist Band. To obtain the desired

spectrum layout, a possible solution would be reversing one of the components (either I or Q). This means that the same IQ sequence could not be used to generate the same spectrum layout in both the first and second Nyquist Bands. The NCOs in Proteus can be set to frequencies over the Nyquist Frequency so the right frequency will be directly obtained in the second Nyquist Band. Additionally, the behavior of the lockup tables which are used to generate the ***cos*** (for the I multiplier) and ***-sin*** (for the Q multiplier) carriers become, for the first Nyquist band, in ***cos*** and ***sin*** functions, respectively. This means that the Q component is reversed by this process and the same IQ stream will produce the same spectrum layout no matter the image being used just by setting the NCO to the final carrier frequency.

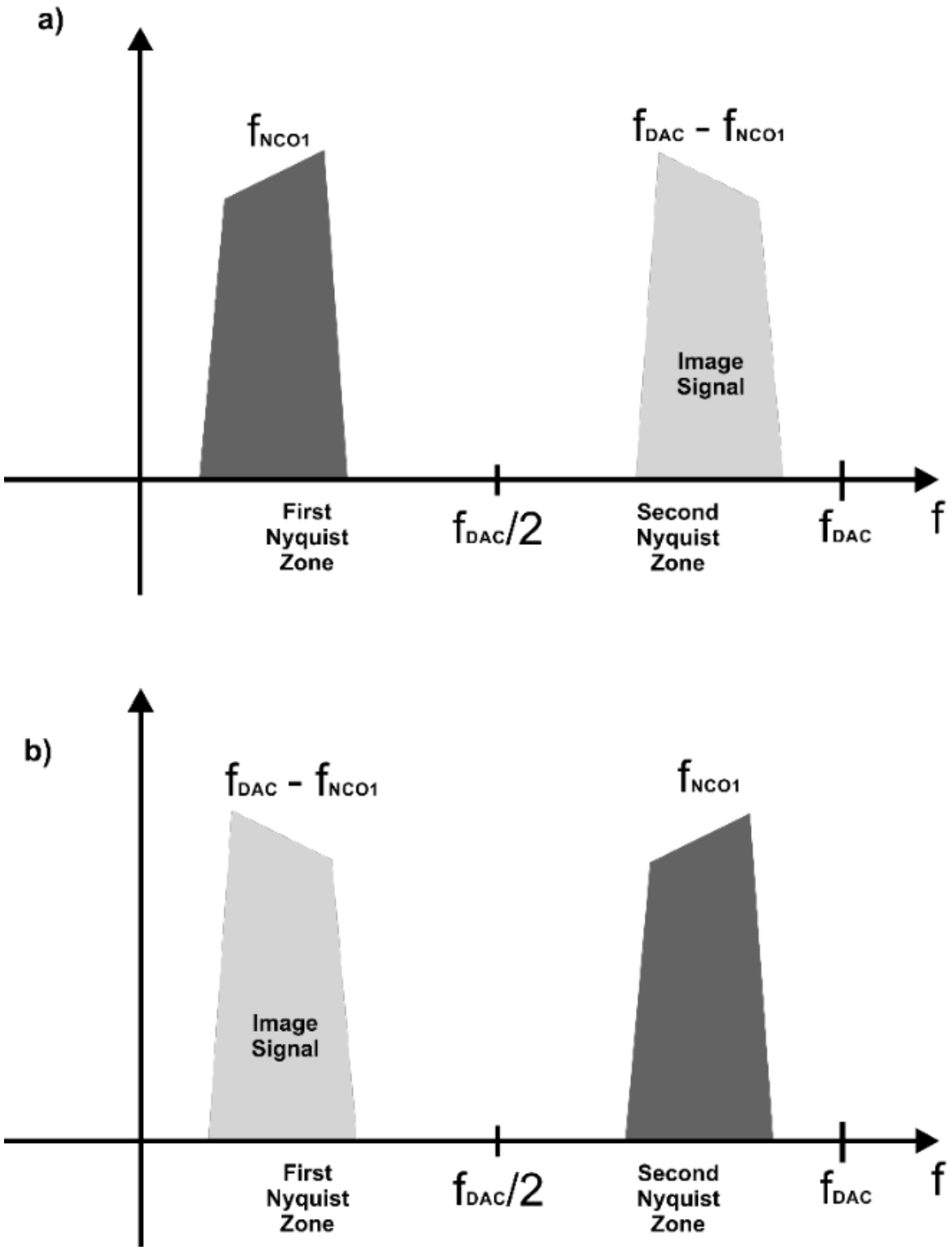

Figure 8.5 I/Q Effects of Setting the NCO Frequency within the First (a) and the Second (b) Nyquist Band for the IQ Modulated Signals

8.4 TWO Mode

In the 'TWO mode, two different IQ streams are applied to each IQ modulator stage associated to each channel so two different modulated signals will be generated concurrently at two designated bands according to the frequencies set for the two associated NCOs, Figure 8.2 c). Initial phase for each NCO can also be set to any desired value. When multiple channels are set to the same frequency, the relative phase between those channels can be defined so any set of signals for applications such as MIMO, Beamforming, or Phase Array (AESA) Radar can be easily implemented. As in the 'ONE' mode, the two IQ pairs must be stored and transferred together to the waveform memory. Both sets of I and Q waveforms, once calculated, must be quantized and interleaved to build the combined waveform to be downloaded to the selected segment.

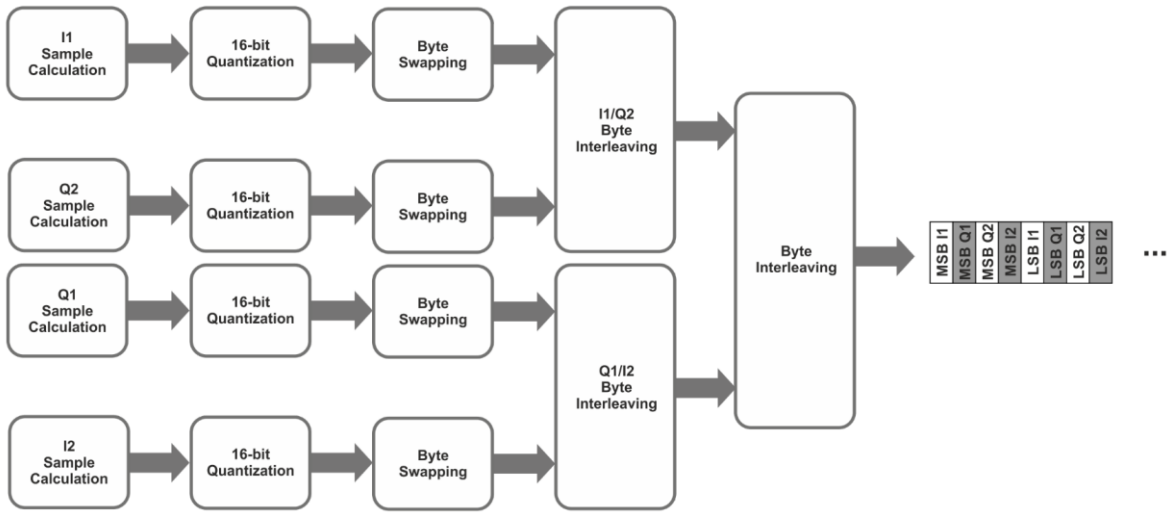

Figure 8.6 I1/Q1/I2/Q2 Sample Processing for Download to the Waveform Memory in Proteus Working in the DUC 'TWO' mode

Although each IQ pair can be defined independently, all these waveforms must share the same sample rate and number of samples as they will be handled as a single entity. Waveform length granularity conditions still apply to the two complex interleaved IQ waveforms, so the number of the complex samples before interleaving must be a multiple of one fourth (1/4) of the granularity for the generator. Baseband waveforms must be calculated at the right sampling rate, equal to the DAC's sample rate divided by the interpolation factor. Interpolation factor can be chosen among the 1X, 2X, 4X, 8X, and 16X choices. Not all the interpolation factors are valid for every sample rate as the effective 16-bit sample transfer rate from the waveform memory cannot be higher than 2.5 GS/s for each channel. Effective sample rate from the waveform memory is four times the sample rate for the baseband complex waveform. The available modulation bandwidth for the 'TWO' mode is half the one for the 'ONE' mode. Table 8.1 shows the maximum DAC sample rate that can be set for a given interpolation factor. The combination of DAC sample rate and interpolation factor must be selected in such a way that the complete spectrum of the modulating signal can be accommodated within the available Modulation Bandwidth.

The same considerations about the NCO frequency settings and the way to generate signals in the first and second Nyquist bands shown in the previous section for the 'ONE' mode, apply for the 'TWO' mode. However, in the 'TWO' mode it is possible to generate two modulated signals in different Nyquist bands. When doing so, it is important to select the right DAC sample rate so the unwanted images in the other Nyquist bands do not interfere with the wanted ones.

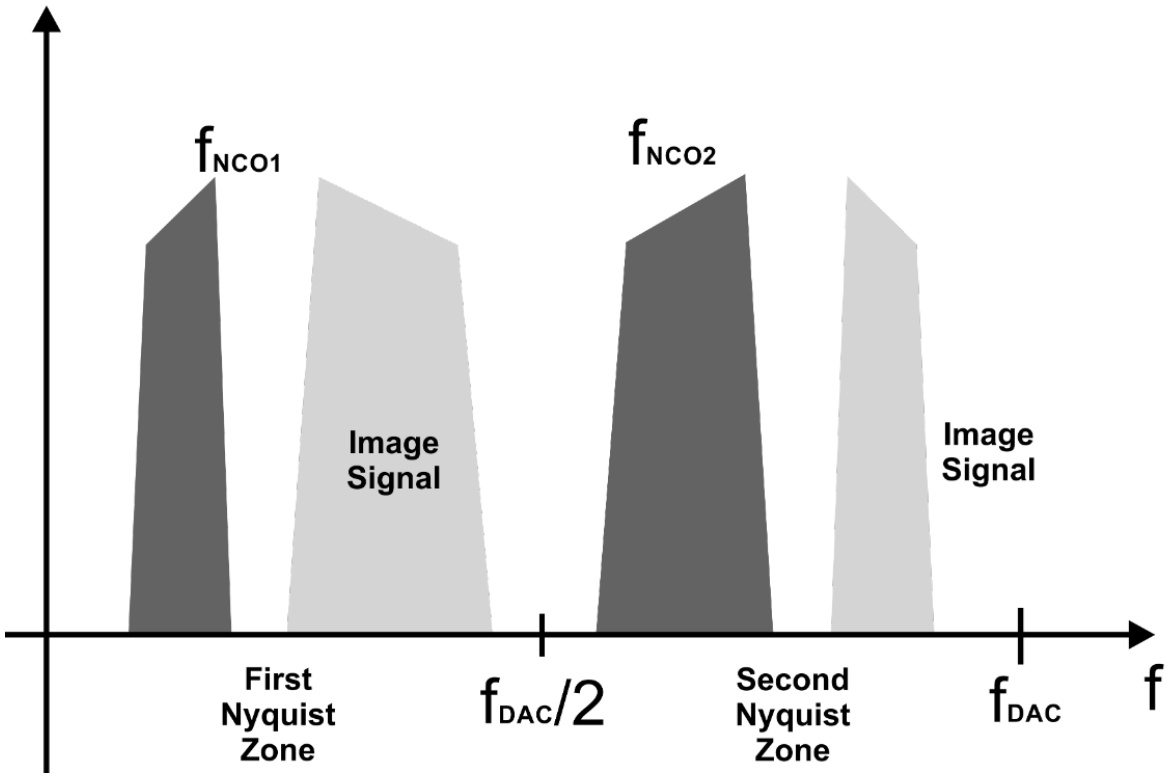

Figure 8.7 Generation of Two Modulated Signals Located in Different Nyquist Bands in the "TWO" Mode

8.5 HALF Mode

In the previously described modes ('ONE' and 'TWO) baseband IQ waveforms are stored and transferred from the waveform memory as a single entity through the interface between the waveform memory and the conversion block for each channel. In the 'HALF' mode, this limit is overcome by using channel pairs (the ones associated to the same waveform memory such as CH1 & CH2) and half of one of the IQ modulators in the DUCs associated to those channels, Figure 8.2 2d). The odd numbered channel of the pair will be assigned to the I component while the even numbered channel will be associated to the Q component. The NCOs for those two channels will be set to the same frequency while the relative phase of the carriers generated by them will be 90 degrees apart. In order to avoid any impairment caused by differential delays, skews, or frequency response between the analog outputs of the participant channels, the numerical modulated output from the second channel is internally routed to an adder associated to the first channel and the combination of both waveforms is supplied to the DAC of the first channel. The available number of output channels in this mode will be half, but the available sampling rate (and modulation BW) will be twice the one for the 'ONE' mode. As each component is transferred to a different channel processing block, the I and Q waveforms are defined and transferred as independent entities as regular waveforms. Each component, once calculated, must be transferred sequentially to two different segments in the shared waveform memory. Users must set the same frequency for the primary NCO for each channel. However, the right 90 degrees relative phase is set automatically by Proteus.

The same considerations about the NCO frequency settings and the way to generate signals in the first and second Nyquist bands shown in the previous section for the 'ONE' and 'TWO' modes, apply for the 'HALF' mode. However, a different method to reverse the spectrum of the output signal is available for the 'HALF' mode. This method consists in swapping the segment assignments for the two participating channels. Swapping the I and Q components in a quadrature (IQ) modulator is equivalent to reverse the spectrum.

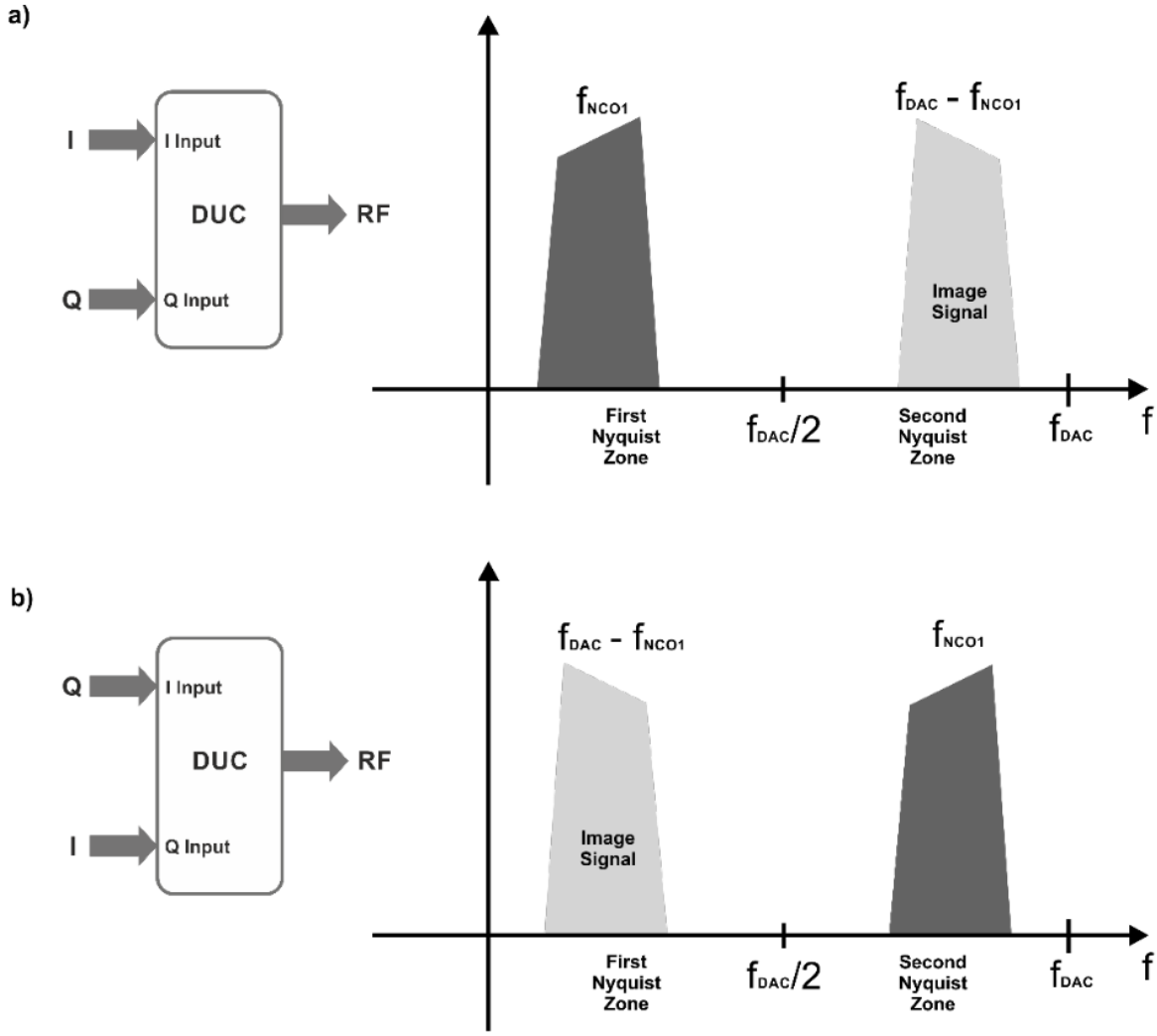

Figure 8.8 Alternative Method of Reversion of the Spectrum for the "HALF" Mode

8.6 Waveform Normalization

IQ waveforms are defined as 16-bit samples just as regular waveforms are. As seen in the previous sections, waveform data must be formatted in the proper way for each DUC mode. In the direct modes, just keeping samples in the 0-65,535 range is enough to make sure no DAC clipping will occur. This is not the case for the DUC modes. I and Q samples are multiplied separately by quadrature carriers and the output of the multipliers are added before being supplied to the DAC. As the output of each multiplier can go from 0 up to 65,535 (15-bit arithmetic), nothing guarantees that the output of the adder will not exceed the limits of the DAC. A careful analysis of the way a quadrature modulator works shows that for a -1.0/+1.0 normalized I and Q components, the

maximum (worst case) output of the adder will be -1.4142/+1.4142. This means that to avoid DAC clipping, the combined amplitude of the modulation vector must be 1.0. One way to make sure this is the case, is normalizing both waveforms at a time so the maximum magnitude of the modulation vector is 1.0, Figure 8.9 9a). This is the way to make the best possible usage of the DAC dynamic range. Proteus incorporates a +6dB gain stage in the digital process chain for the DUC. A simple way to make sure that any I and Q waveforms will never clip is by deactivating the 6dB gain for any each IQ modulator in any particular DUC. This is not optimal for the 'ONE' and 'HALF' modes as it will result in a 6dB attenuation of the waveform when it is enough with 3dB. However, this is just right for the 'TWO' mode, Figure 8.9 9b).

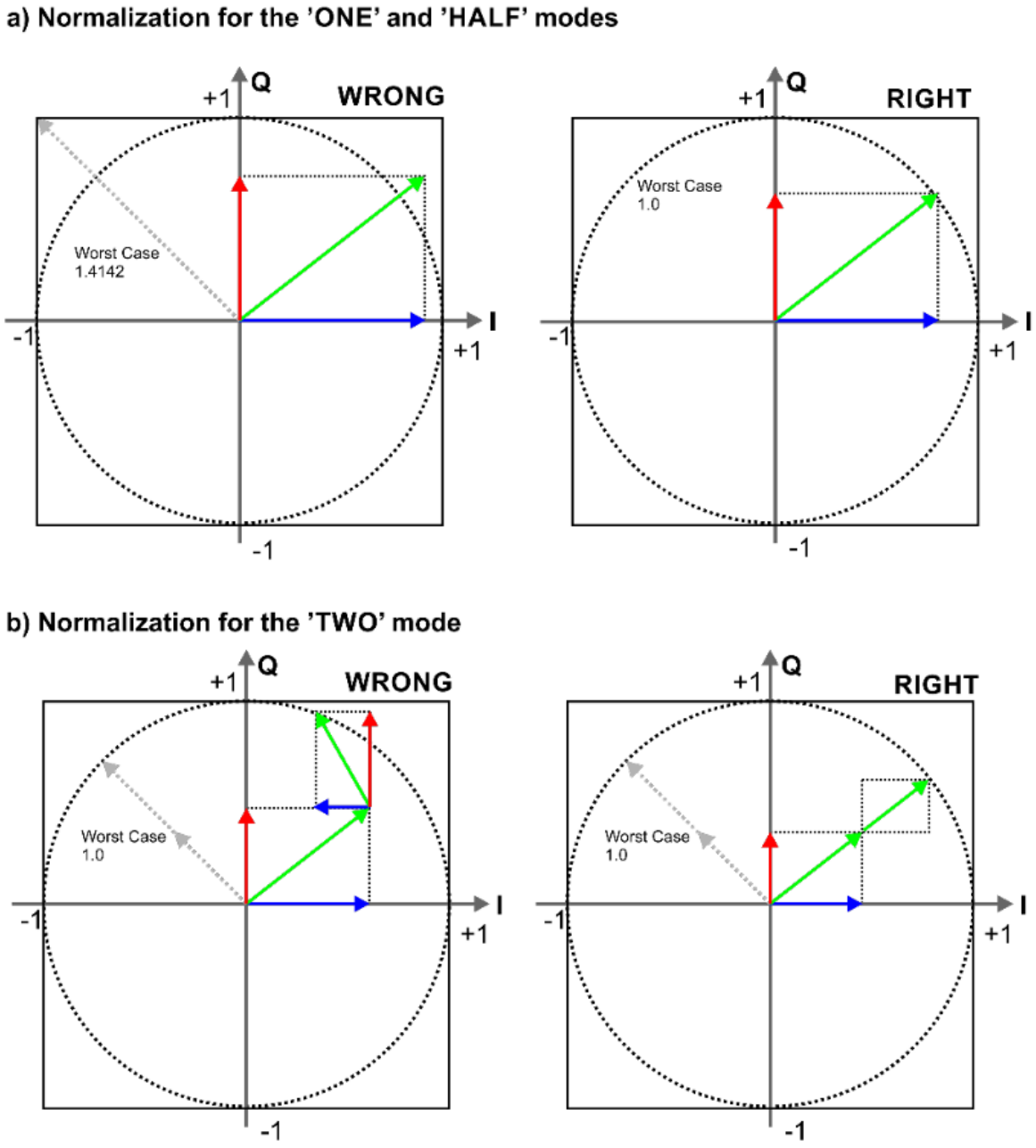

Figure 8.9 IQ Sample Normalization for the "ONE" and "HALF" Mode (a) and the "TWO" Mode (b)

Waveforms in Proteus are defined as unsigned 16-bit integers. However, these waveforms are handled by the DUC processing chain (interpolators, filters, multipliers, adders) as signed integers with the 32,768-level corresponding to the 'zero' level. Typically, normalized waveforms in the -1.0/+1.0 range are mapped to the 0/65,536 range. When doing so, the 0.0 level does not correspond exactly to the 32,768 level and, therefore, the final waveform will have a tiny additional DC component. For direct conversion, this is not typically an issue as this component is either unnoticeable, or it may be removed by a DC-block stage, or it can be corrected through the usage of the Offset control. However, for the DUC modes, the DC component caused by the typical full DAC mapping will show up as a small residual carrier that cannot be removed through any of the previously described methods. To avoid this issue, normalized waveforms should be mapped to the 1/65,535 range instead of the traditional 0/65,535 range.

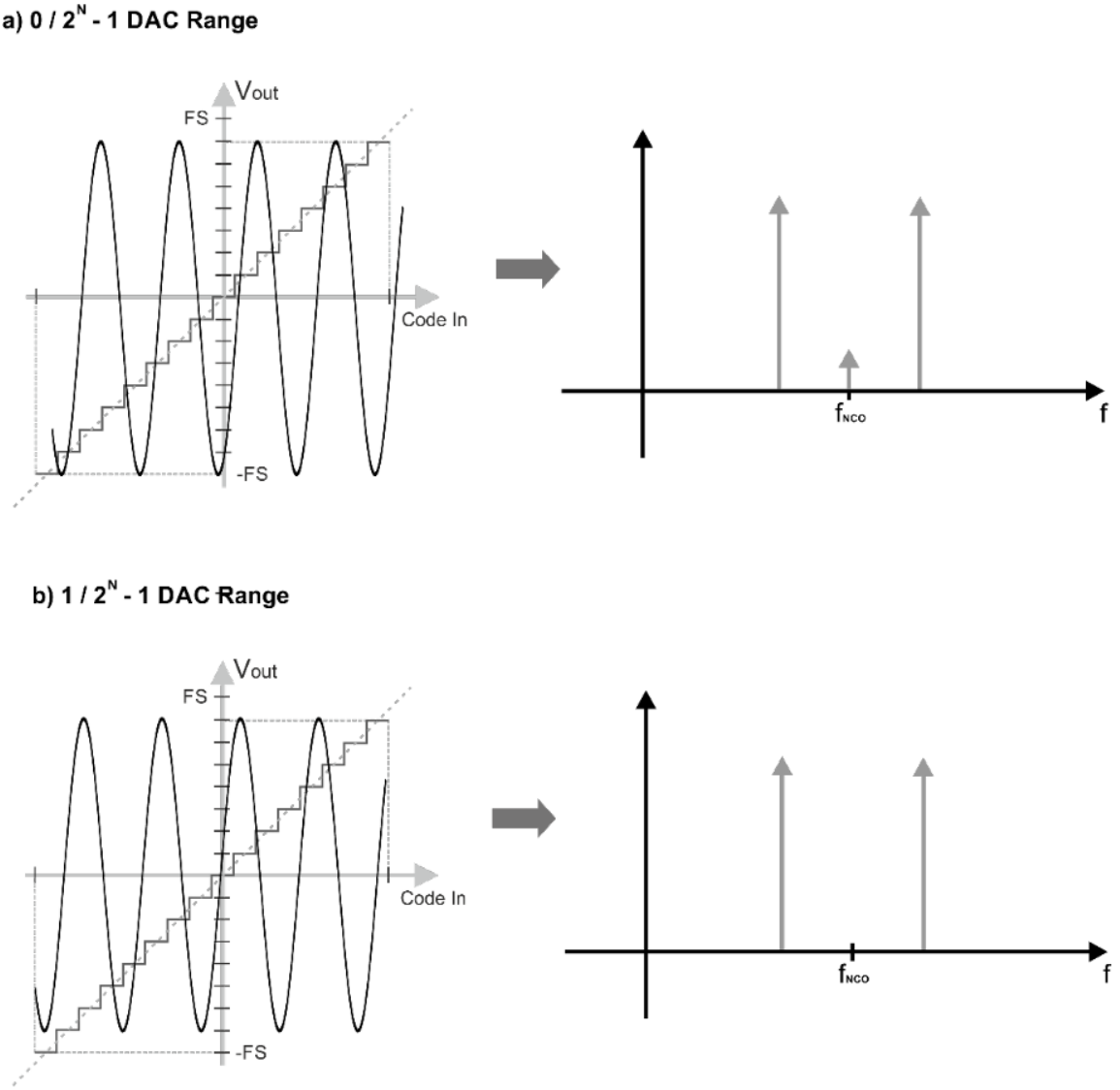

Figure 8.10 DAC Range Adaption to Avoid the Residual Carrier Impairment in the Output as Seen in (a)

9 Triggering System

9.1 Introduction

The ability to program and control what is being generated from the AWG requires two basic functionalities. The first is being able to program the memory segments with the desired waveform data to be generated, as was explained in chapter 5 Arbitrary Mode. The second functionality is being able to control which segment or task is to be played out and when.
The simplest way to generate a waveform or task table is simply to program it in advance, as explained in the Arbitrary and Task mode chapters. The waveform or task table will be generated continuously once the output is switched on. However, in many applications, the exact timing of the generation of each waveform or task needs to be controlled. For this reason, there is a triggering system, where various signals, internal or external can be used to apply certain conditions to the waveform generation.
In this chapter we will explain how the triggering system works and its capabilities.

9.2 Trigger Run Modes

As explained previously the Proteus device has two operation modes, Arbitrary and Task. Trigger functionality is applied differently depending on the operation mode of the instrument.

9.3 Arbitrary Mode

When operating in arbitrary mode the Proteus device has two run modes, continuous and trigger.
In continuous run mode the waveform stored in the selected segment is available at the output terminals when the channel output is turned on. The selected segment is played continuously and will continue until a different segment is selected, the output is turned off or the run mode is set to trigger.
Once the device is set to trigger run mode the trigger is armed and is sensitive to the input signal or bus commands depending on the trigger source. At the channel output an idle waveform is generated. The idle waveform can be selected by the user and the available options are explained in section 9.7 Output Channel Trigger Settings.

9.4 Task Mode

When the Proteus device is set to task mode, the waveforms are generated according to the task table. As explained in the Task mode chapter the task table is made up of different tasks. Each task in the task table contains multiple parameters, such as enable signal, abort signal and jump condition that define the trigger functionality for the given task. Therefore, in task mode there is no selected run mode but rather each task is played out according the conditions defined.

9.5 Trigger Source

The Proteus AWG module can be initiated to produce waveform functions from several trigger sources.

- Trigger In 1 labelled TRIG 1 (WDS, Trigger, ExternTrig1).
- Trigger In 2 labelled TRIG 2 (WDS, Trigger, ExternTrig1).

- Bus commands that are applied to the instrument (WDS, Trigger, CPU).
- Internal Trigger (WDS, Trigger, InternTrig).
- Digitizer, (Option AWT) (WDS, Trigger, FeedbackTrig).
- Dynamic Jump connector (Option FS) (WDS, Trigger, HwControl).

9.5.1 TRIG 1/2

When activating the external TRIG 1 or TRIG 2 trigger source, every valid signal that is applied to the input connector is stimulating the Proteus device. To define the condition for a valid signal, it is necessary to program the trigger level and trigger slope. The trigger level defines the necessary voltage level that the trigger signal needs to cross for it to stimulate the instrument. While the trigger slope defines whether the trigger input is sensitive to a positive transition or negative transition. The trigger level is defined per trigger input and is common to all channels.

9.5.2 Bus

When selecting Bus as a trigger source, trigger commands from a remote interface are accepted by the instrument.

9.5.3 Abort (Jump) Mode

Until now we have discussed scenarios where the Proteus device is idle and is then triggered. However, there are many applications where the device receives a valid trigger while a segment is being generated. The abort mode parameter enables the user to control exactly how the instrument reacts in such a case.
There are two setting options for the abort mode:

- Eventually – In Eventually mode, the first valid trigger that is received is accepted by the device. However, the current segment that is played is completed before the trigger action is initiated. Any consecutive triggers that are received while the segment is being played are ignored.
- Immediately – In Immediately mode, the instrument does not complete playing the current segment but performs the trigger action on the next clock cycle. Any consecutive valid trigger that is received is accepted and the programmed trigger action is executed.

9.5.4 Internal Trigger

An additional source for trigger generation is the internal trigger. There are two operating modes in this state:

- In periodic mode, an internal time counter is generating trigger pulses every specific time elapsed. It is the user responsibility to ensure that the generated trigger will not interrupt wave generation before its end.
- In delay mode, the user sets the number of clocks which will generate a trigger after the wave generation ends. TBD

9.5.5 Digitizer (AWT)

When configured with the AWT option, the digitizer can be programmed so that a valid signal triggers the instrument.

9.5.6 Dynamic Jump Connector (DJ)

When configured with the DJ option, the valid signal on the dynamic jump connector can be set to trigger the instrument.

9.6 Trigger Source Attributes

For each trigger source the user can program certain attributes. These attributes constitute what is the trigger state and what is a valid trigger signal. All the trigger source attributes except trigger level are channel dependent and can be different for each of the instrument's channels.
The trigger source attributes are described in the following paragraphs.

9.6.1 TRIG ½

External trigger inputs TRIG1 and TRIG2 have the following attributes:

- Trigger State – Enables or disables the trigger state for the specified channel. When trigger state is ON the trigger input is armed for the active channel. When turned off the trigger input is inactive and ignores all trigger signals.
- Trigger Type – Selects between the type of trigger signal. Edge defines the valid trigger on the transition of the trigger signal. Gate type trigger signal outputs the waveforms on a stable gate level between two gate transitions. The gate opens on the first positive trigger transition and closes on the next negative transition.
- Trigger Polarity – When the selected trigger type is Edge user can set whether trigger is initiated on the rising edge or falling edge of the trigger signal

Trigger Pulse Detect Width – The trigger pulse detect width sets the width of a valid trigger signal in units of time. User sets a time interval during which the trigger signal valid level must be kept in order for the trigger signal to be valid.

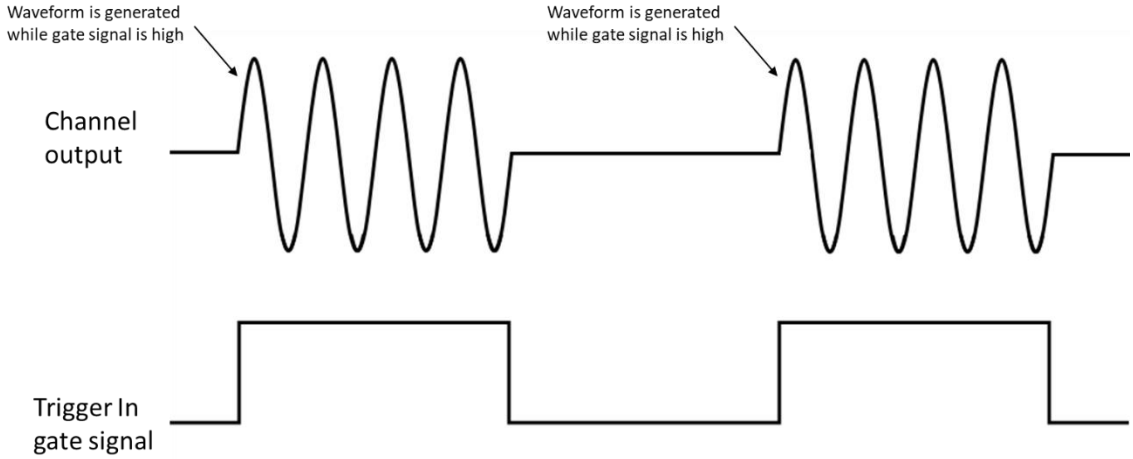

Figure 9.1 Output Signal with Gate Type Trigger

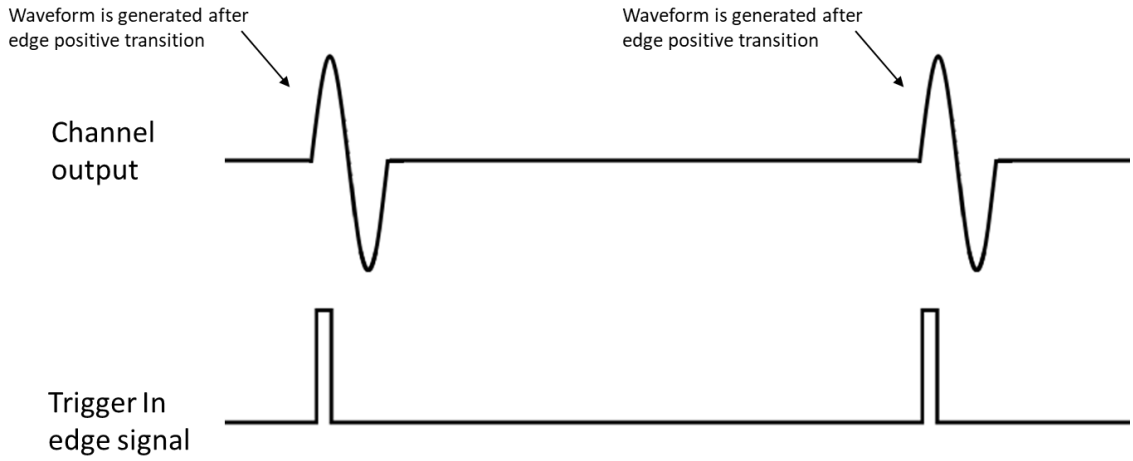

Figure 9.2 Output Signal with Positive Edge Type Trigger

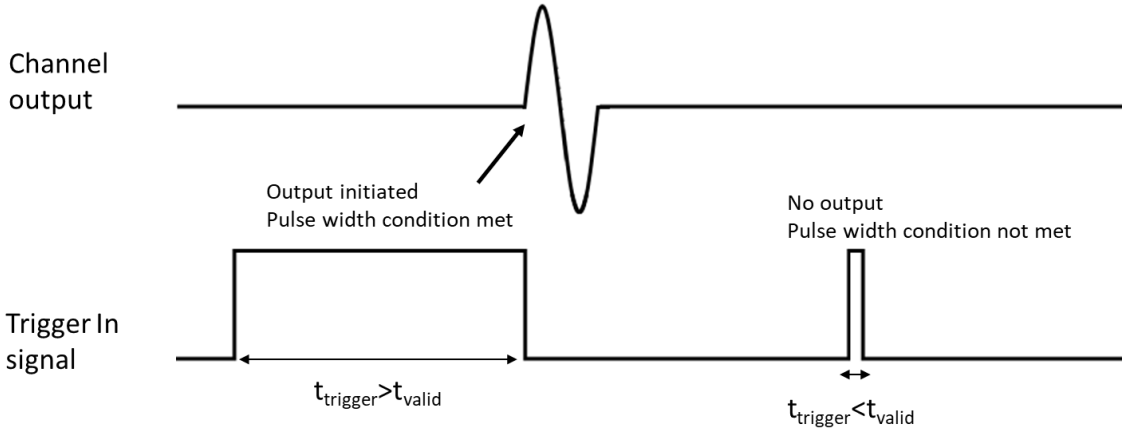

Figure 9.3 Outputs Behavior with Pulse Detect Width Set to Time t_{valid}

9.6.2 Internal Trigger

The internal trigger generator operates as a free running asynchronous trigger generator. It may be used for applications that require periodical and constant generation of output cycles, or to replace external trigger devices. The following attributes can be programmed:

- Trigger State - Enables or disables the trigger state for the specified channel. When trigger state is ON the internal trigger generator is active channel. When turned off the internal trigger generator is inactive.
- Trigger Period – Sets the time period between triggers for the internal trigger generator.

Note

- In order to prevent errors, the period of the internal trigger must be larger than the period of the output waveform.

9.7 Output Channel Trigger Settings

The trigger source attributes define the state of the trigger source and the conditions for a valid trigger signal. Once those are defined it is necessary to define the behavior of the instrument once a valid trigger signal is received. The following paragraph describe the parameters that can be defined to control the instrument response to a valid trigger signal.

9.7.1 Enable (Start) Source

The enable source defines which trigger source starts the waveform generation. User can set any one of the available trigger sources as the source for initiating waveform generation.

Note
In arbitrary mode one of the trigger sources must be set as the enable source. If set to none the unit will not output any waveform in trigger mode.

9.7.2 Disable (Abort) Source

The disable source defines which trigger source aborts the waveform generation. User can set any one of the available trigger sources as the source for aborting waveform generation.

9.7.3 Idle Waveform

When the channel output is waiting for a trigger the output must still generate a waveform. This waveform is referred to as the idle waveform. User can select between 3 idle waveforms:

1. DC – the output is a DC waveform. The DC level can be programmed as explained in the following paragraph.
2. FirstPoint – The output is a DC waveform of a level that is equivalent to the first point of the segment to be generated.
3. CurrentSeg – The output is the waveform programmed to the current segment.

9.7.4 DC Level

When the idle waveform is set to DC, the DC level parameter enables the user to program the required DC level of the idle DC waveform. The level is programmed in value of DAC bits and enables the users to select any DC level as the idle level of the channel output while waiting for a trigger.

9.7.5 Loops Count

Once the Proteus device receives a valid trigger signal to generate a segment the user can program the number of times that segment is to be repeated. The number of repetitions, or loops, is set in the Loops Count parameter.

Note
When the loops count is set to 0 the segment will be repeated infinitely until it is aborted.

9.7.6 Low trigger Jitter(LTJ Option)

A trigger signal, whether it comes from an external source or from an interface command, is routed through electrical circuits. These circuits cause a small delay known as system delay. System delay cannot be eliminated completely. System delay is a factor that must be considered when applying a trigger signal. It defines the time that will lapse from a valid trigger edge or software command to the instant that the output reacts.
In case of a trigger signal that is asynchronous to the device system clock, an additional variant delay called trigger jitter is added to the system delay. The trigger jitter is defined as the variation in time of the triggered signal position with respect to the triggering signal.
Trigger jitter adds uncertainty to the generated signal. This can be a very critical parameter in many applications and experiments that need the generated signals to be very near or completely deterministic.

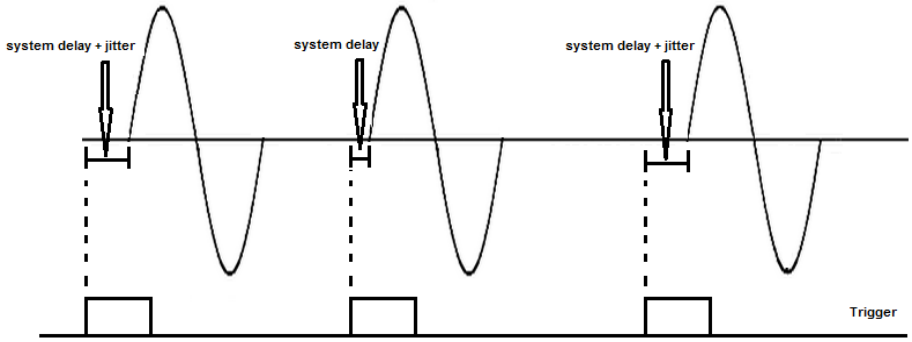

Figure 9.4 Trigger Jitter and System Delay

The Proteus series offers several options on how to minimize the trigger jitter. For asynchronous trigger signals there is the Low Trigger Jitter option. This option can be added when ordering your Proteus device. Using this option can reduce the trigger jitter by a factor of more than 10. To activate the option user simply needs to turn the low trigger jitter state to ON.

Note
Activating the low jitter option reduces the trigger jitter however the system delay is increased.

9.8 Minimizing Trigger Jitter

As discussed in the previous section when stimulating the Proteus device with a trigger that is asynchronous to the system clock, user can minimize the trigger jitter by enabling the low trigger jitter option. However, in many applications in order to minimize the trigger jitter even further the trigger signal and triggered instrument are synchronized.
One option is to feed the same reference signal to both triggering and triggered instruments. However, the Proteus device offers the CLK OUT signal. When this signal is used as the triggering device clock it guarantees the lowest attainable trigger jitter.

10 Digitizer

10.1 Introduction

The digitizer block in the Proteus AWT (Arbitrary Waveform Transceiver) platform adds the capability of receiving analog signals and converting them to digital waveforms. The basic characteristics of the digitizer block are the following:

- One digitizer block (2 channels) per PXIe module or per benchtop/desktop unit.
- Analog BW up to 9GHz.
- User-selectable 2 channels at 2.7GS/s or 1 channel at 5.4GS/s using internal interleaving of both ADCs. Sampling rate can be set by the user over a wide frequency range.
- 12-bit of vertical resolution.
- Three user selectable sensitivity levels HIGH (500mVpp), Medium(400mVpp), and LOW (250mVpp).
- Flexible and powerful internal and external triggering functionality including triggering by level, interval, event counter, and bi-directional cross-triggering between the AWG and the digitizer sections. Trigger events can be defined independently for each channel.
- Single and multiple frame acquisitions with timestamping for absolute timing analysis.
- Single DDC (Digital Down Converter) per channel in dual (2) channel mode and double DDC in the single (1) channel mode, tunable using a standalone NCO (Numerically Controlled Oscillator) over the full Nyquist Band with complex (I/Q) waveform output.
- Massive acquisition DDR4 memory shared with the AWG block.
- Data generated by the digitizer can be processed in the internal FPGA using the standard processing blocks or user-defined IP.
- WDS application provides digitizer control functions.

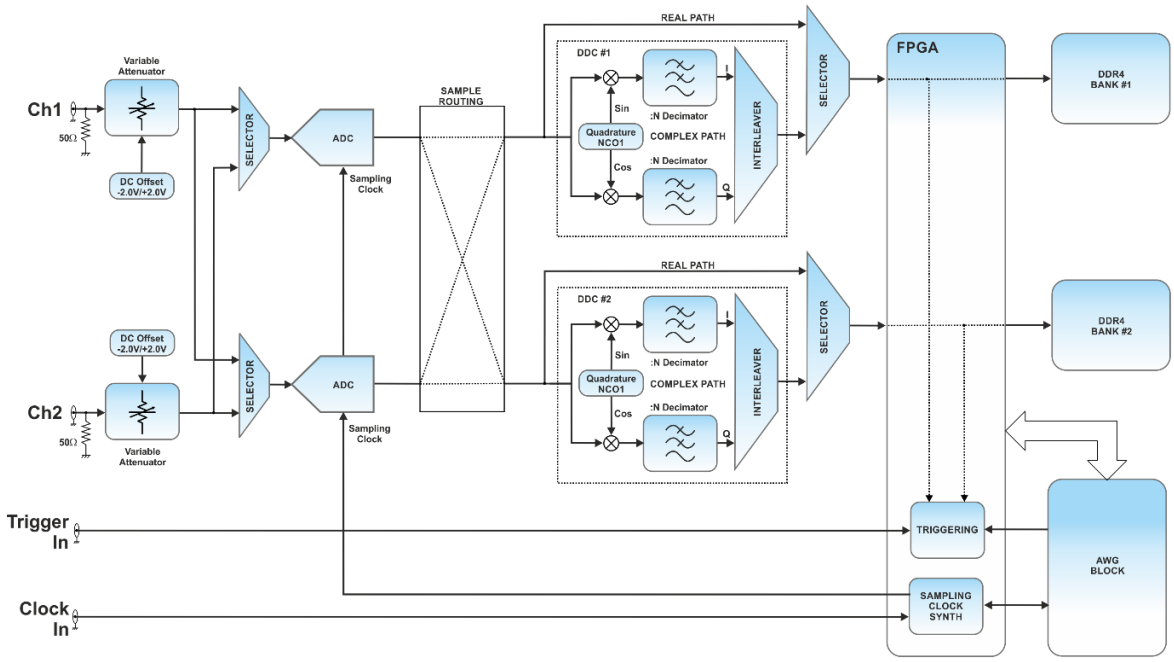

Figure 10.1 Digitizer Section Block Diagram for DUAL Mode

The digitizer block can work independently of the AWG block or together with it. They can share bidirectional trigger and event signals, or even synchronize the operation of the DUC and DDC for coherent, deterministic modulation/ demodulation of RF signals.

10.2 Theory of Operation

The above figure shows the simplified block diagram of the digitizer block in the Proteus platform. In the dual mode, sampling rate is shared by both channels so sampling instants are aligned in time within a very narrow margin. The first stage after the input is a variable attenuator with three different settings so the full-scale voltage can be adapted to the characteristics of the signal, and a DC offset control so the voltage window can be shifted in the -2.0V/+2.0V range. After the attenuator and DC offset block, each ADC block incorporate a S&H (Sample and Hold) circuit. The S&H captures the near-instantaneous voltage level of the input signal for a close to ideal sampling process. This allows for the effective capture of signals located beyond the first Nyquist band and for a flat frequency response over a large frequency band, see the figure below. All signals acquired beyond the first Nyquist band will show up in the acquisition as images in the first Nyquist band. Special care must be taken so signals present in different Nyquist bands do not overlap when under-sampled to the first Nyquist band. It is also important to select sampling rate, so the band occupied by the target signals are not split among multiple Nyquist bands.

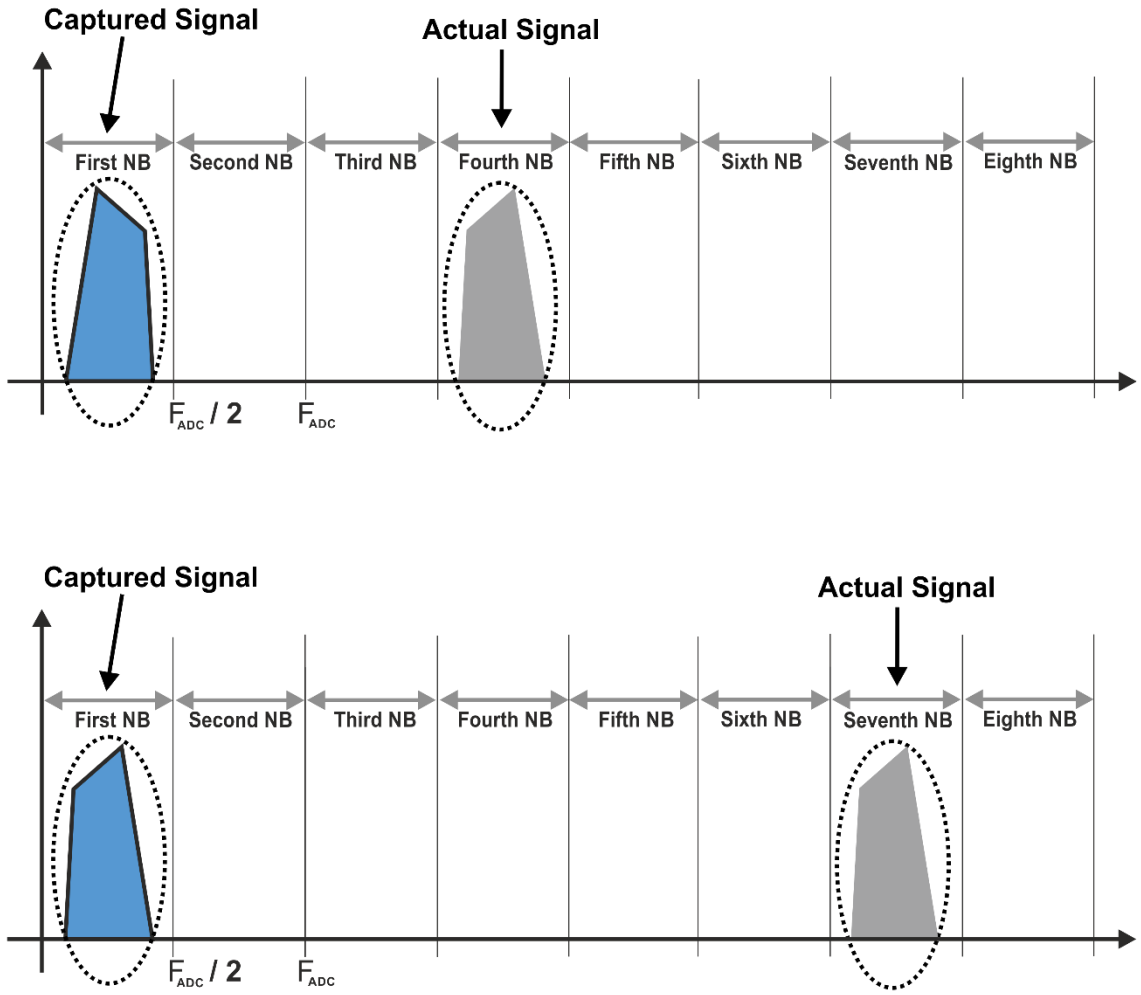

Figure 10.2 Capturing Signals Beyond 1st Nyquist Band

The S&H stage is connected to the 12-bit ADC (Analog to Digital Converter). Samples produced at the sampling rate are organized as 48-samples blocks for transfer to the acquisition memory. Therefore, the number of samples in a single frame must be a multiple of 48. The acquisition memory for the current frame is organized as a FIFO (First In First Out) buffer so when the trigger event occurs, acquisition is stopped after a given number of samples defined by the user. In this way, information before and after the trigger event may be captured. The closest sample to a trigger event is located in an around 48 samples region close to the nominal trigger sample location. When operating in the SINGLE mode, only channel 1 input is operational. The same signal is applied to both S&H stages, but the sampling instant is delayed by half the sampling period. In this way, by interleaving the two DACs, is equivalent to using a DAC with twice the sampling rate, see below figure.

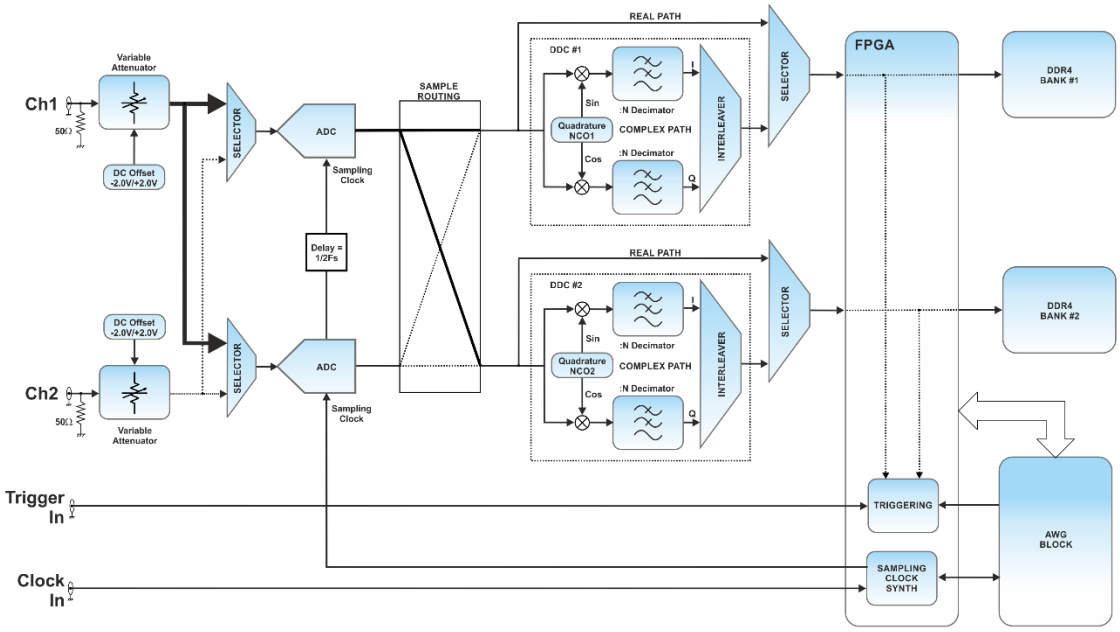

Figure 10.3 Digitizer Section Block Diagram for SINGLE Mode

The acquisition memory is shared with the AWG block. The AWG block can use samples up to 16-bit wide. As the digitizer in the real (direct mode) produces 12-bit samples, they are stored as 4 samples every 3 x 16-bit words, so memory efficiency is improved by 25% when compared to storing one 12-bit sample for every 16-bit word. Digitizer's CH1 is connected to the DDR4 memory bank shared by the AWG's CH1 and CH2 while Digitizer's CH2 is connected to the one shared by AWG's CH3 and CH4. In the P9082M module, Digitizer's CH1 and AWG's CH1 share one of the memory banks, while Digitizer's CH2 and AWG's CH2 share the other one. This is also true for the SINGLE mode although the interleaved samples (odd samples in bank #1 and even samples in bank #2) are always handled as a single logical entity so they are transferred to the controller without requiring any further formatting or interleaving.

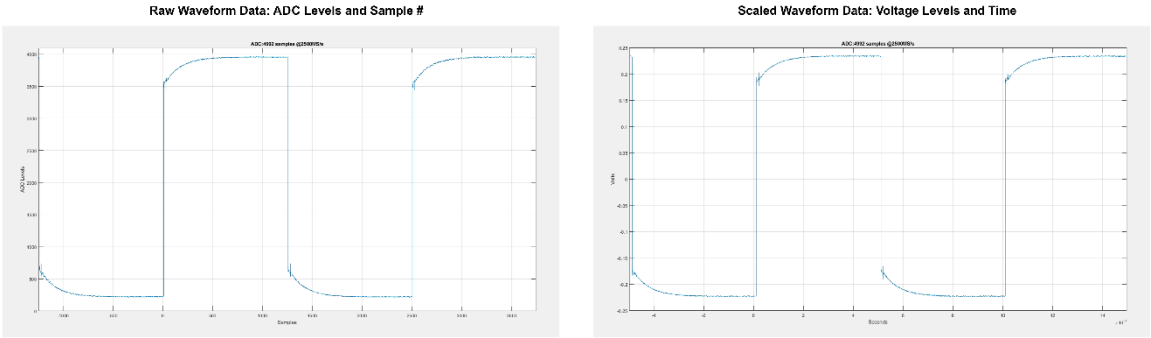

Figure 10.4 Waveform Before (Left) and After (Right) Proper Voltage and Time Scaling

Actual voltage level (VL) for each sample in a waveform can be calculated from the acquired waveform data (DL) by using the following expression:

$$VL(n) = (DL(n) - 2048) \times FS / 4096 + VOFF$$

FS = Full Scale Voltage, VOFF = Voltage Offset for the ADC

Actual relative to the trigger timing (T) can be obtained for each sample from the pre-trigger (PT) and Sample Rate (SR) settings by using the following expression:

$$T(n) = (n - PT) / SR$$

Timestamping can be used when absolute timing information is required. Timestamping adds one piece of information that may be required in some tests, in order to check absolute, high-resolution timing for all the frames so timing between events and samples can be recovered from acquisitions.

10.3 Working Modes

The Digitizer section can work in two different modes regarding the number of enabled channels:

- Dual: In the dual mode, all the digitizer channels are operative. Sample rate can be set in the 800MS/s – 2.7GS/s range. Acquired waveform length must be always a multiple of 48 samples (Figure 10.1 Digitizer Section Block Diagram for DUAL Mode).
- Single: In the single mode, only the odd numbered Digitizer channels are effective while sample rate can be set in the 1600MS/s – 5.4GS/s. The ADCs from both channels are combined in a single interleaved DAC effectively doubling the sampling rate. As acquisitions are handled internally as two acquisitions in parallel, acquired waveform lengths must be a multiple of 96 samples (Figure 10.3 Digitizer Section Block Diagram for SINGLE Mode).

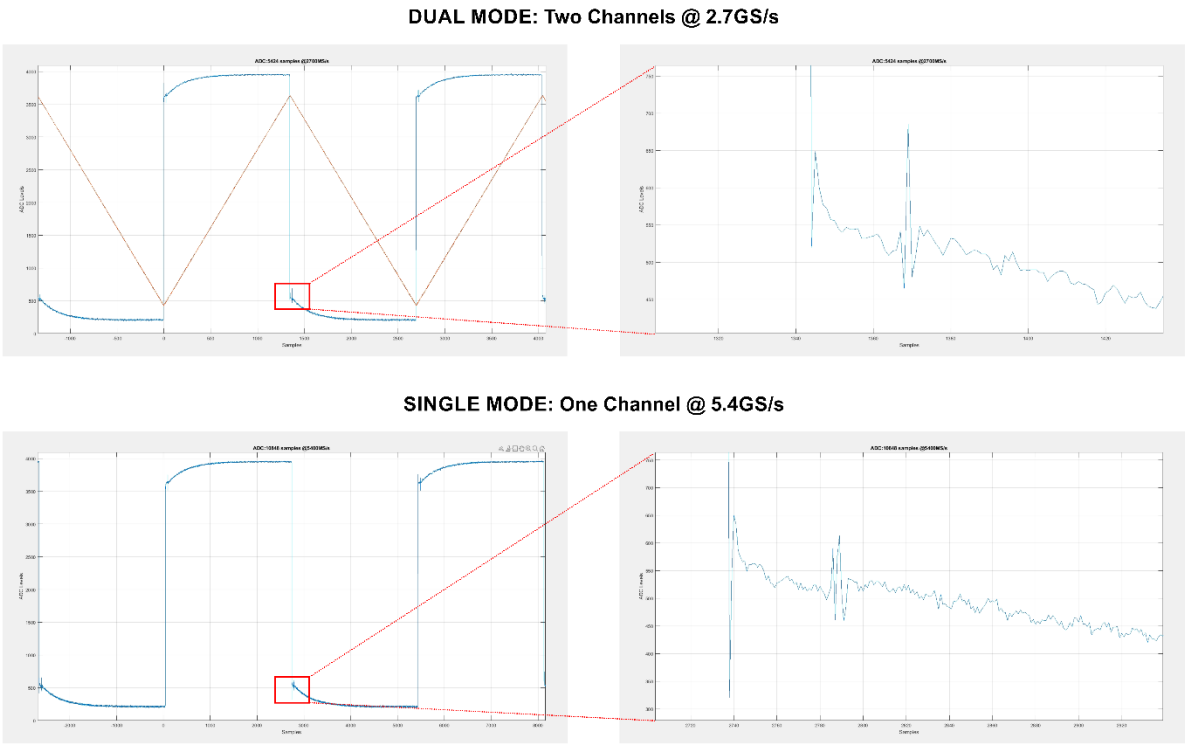

Figure 10.5 Dual Mode (Two Channels, Half Sample Rate, Top) vs. Single Mode (One Channel, Bottom) Acquisitions

The Digitizer section can work in two modes as well when looking to the usage of the DDC (Digital Down Converter):

- Real: Direct acquisition to the waveform memory of the real-only digitized samples at the conversion rate specified by the sampling clock.
- Complex: In the complex mode, each channel activates a DDC that down-converts a limited band of the acquired signal to a complex, decimated (x1, x4, and x16) waveform. Each complex sample is made of two regular samples (real and imaginary, or I and Q) so the amount of effective waveform memory is twice the number of complex samples being acquired. In the single mode, both DDC blocks can be applied to the input signal if sampling rate is equal or lower than 2.7GS/s. Refer to 10.7 DDC Operation for more details.

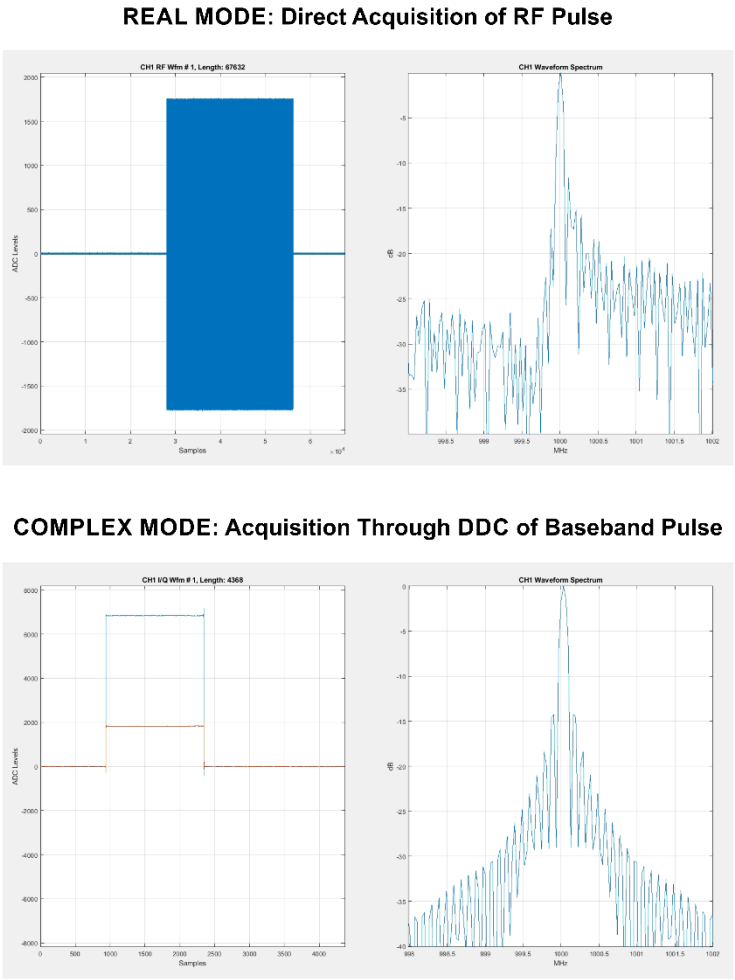

Figure 10.6 Direct Mode (Top) vs. DDC Mode (Bottom) Acquisitions of an RF pulse and the Corresponding Spectrums

10.4 Acquisition Modes

The Proteus digitizer provides a very flexible and powerful acquisition architecture. Acquisitions are made of one or multiple frames of user-defined length. The digitizer starts capturing samples as

soon as it is enabled, and each frame works as a FIFO for the corresponding acquisition. The structure of a frame is shown in the figure below.

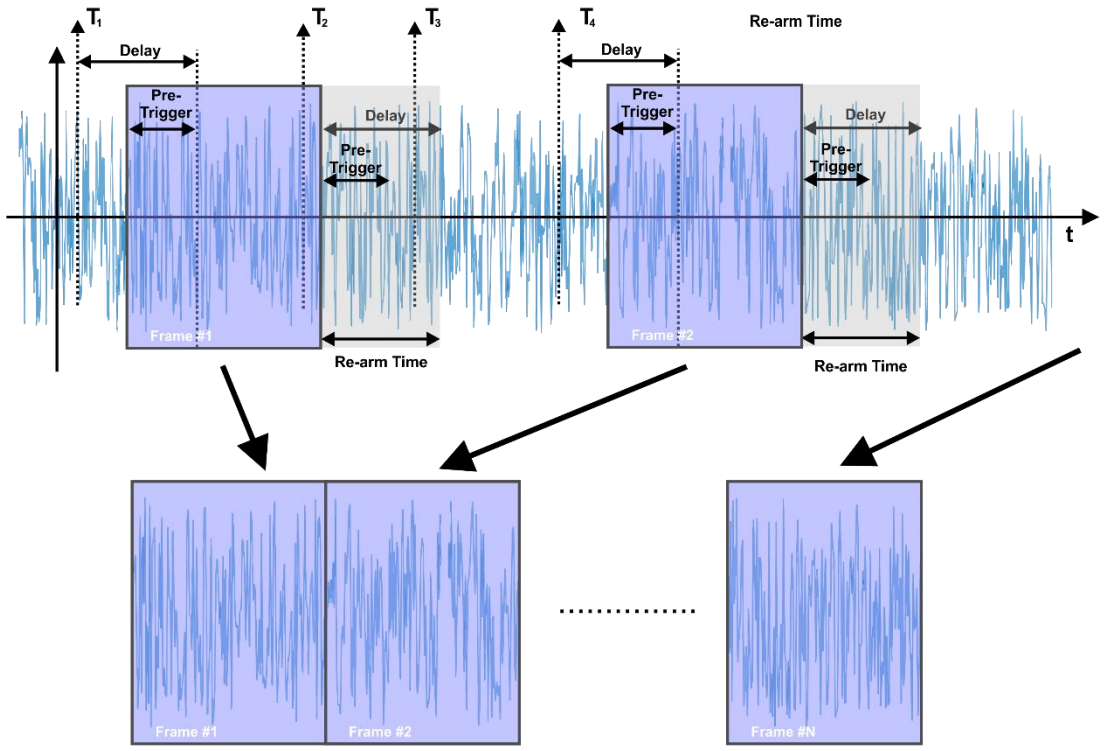

Figure 10.7 Structure of a Multi-Frame Acquisition

The position of the trigger event can be set at any convenient location so important information that happened before the trigger event is not lost. The amount of pre-trigger data is limited by the size of the frame. However, the time window can be located at any time after the trigger event (see 10.5 Trigger Modes for details) applying any convenient trigger delay. This is the sequence of actions for the acquisition of a frame:

1. The acquisition memory configured as a FIFO starts being filled by the incoming samples.
2. The trigger is armed immediately after all the pre-trigger samples are acquired and the current trigger delay can be met. This means that trigger events happening before this instant will not have any effect.
3. An internal counter counts the number of sampling periods to complete the post-trigger acquisition and the trigger delay to effectively stop the acquisition.
4. Immediately, the digitizer jumps to step #1 for next frame's acquisition. This process continues until the designated number of frames are acquired or the acquisition is aborted by the control program.

The acquisition process can be monitored by accessing the acquisition status information using the SCPI command ***:DIGitizer:ACQuire:STATus?***. It is in a comma separated string with four integers with the following format:

`<frame-done>,<all-frames-done>,<pulse-counter-busy>,<frames-count>`

The first three fields can be either '1' or '0' while the last field returns an integer with the number of frames acquired so far. Using field #2 and #4, it is possible to synchronize with the acquisition process and check if it is being performed in an acceptable or normal manner. Monitoring the

number of frames already captured can provide information about the rate of trigger events so it is possible to exit the process after some user defined time-out avoiding waiting for longer than expected.
Although the number of frames is defined with a single command, it is possible to activate the acquisition for a limited number of frames as the first frame and the number of frames for a capture can be defined within the allocated waveform memory. This allows to control the acquisition of chunks of frames according to the needs of the tests being performed. Once all the frames have been acquired or right after aborting acquisition, waveform data can be read from the waveform memory. Data can be read at once or selecting a given section of consecutive frames (see SCPI command ***:DIGitizer:DATA:FRAMes <1st-frame>,<num-frames>*** for details of data formats).
Some acquisition parameters are shared among the channels in a single Proteus module:

- Sample rate
- Frame length
- Number of frames for the current capture

However, trigger settings (including the source and type) can be independently defined for each channel. In this way, both channels can work as a dual-channel oscilloscope where acquisitions for each channel are fully aligned in time, or like two one-channel digitizers as each can acquire their own waveforms independently. Full time correlation may be obtained by recovering the time stamping information, refer to 10.6 Frame Header.

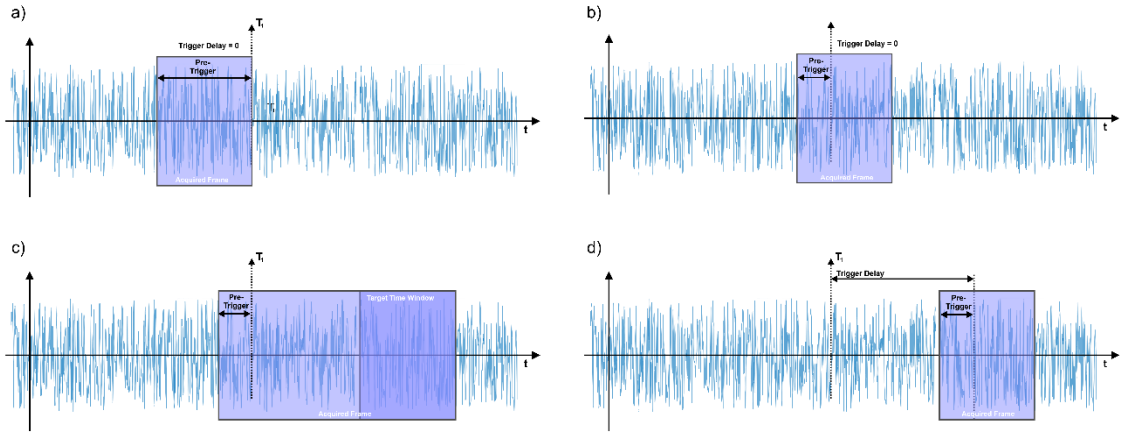

Figure 10.8 Acquisition Window Control

Each frame within an acquisition is defined by its length, the sample rate used in the acquisition, and its position respect to the trigger event that caused the acquisition of that particular frame. The relative position of the trigger event is controlled by two parameters:

- Pre-trigger: This is the number of samples acquired before the trigger takes place. As acquisitions are made using a FIFO architecture, it is possible to capture sections of the signal previous to the trigger event. However, the maximum time before the trigger is limited by the size of the frame itself (Figure 10.5 a). Pre-trigger can be set in such a way that the position of the trigger is located anywhere within the acquisition (Figure 10.5 b).

- Trigger Delay: Sometimes, the target time window can be located away from the trigger event. One possible solution is setting pre-trigger to zero (0) and then setting the frame length to make sure the interesting time-window is acquired (Figure 10.5 c). However, this strategy can result in using the waveform memory inefficiently, limiting the maximum number of frames that can be captured, and an increase in the waveform transfer time. In order to avoid these limitations, it is possible to set a trigger delay, so the effect of the trigger event is shifted by a fixed amount of time (Figure 10.5 d). This trigger delay functionality is available for some of the trigger sources such as the external trigger or the task trigger.

The pre-trigger and trigger delay settings also set a minimum time for the digitizer to effectively arm the trigger to capture a new frame (holdoff or re-arm time) equal to the largest of both parameters measured in time. If a trigger event happens during the holdoff time, it will be ignored (Figure 10.7 Structure of a Multi-Frame Acquisition). Users can set an arbitrary holdoff time as a technique to reject non-wanted trigger events (i.e. to trigger at the beginning of a burst and not in the middle of it). However, this holdoff time will include the minimum holdoff time described in this paragraph (see more details in section 9 Triggering System).

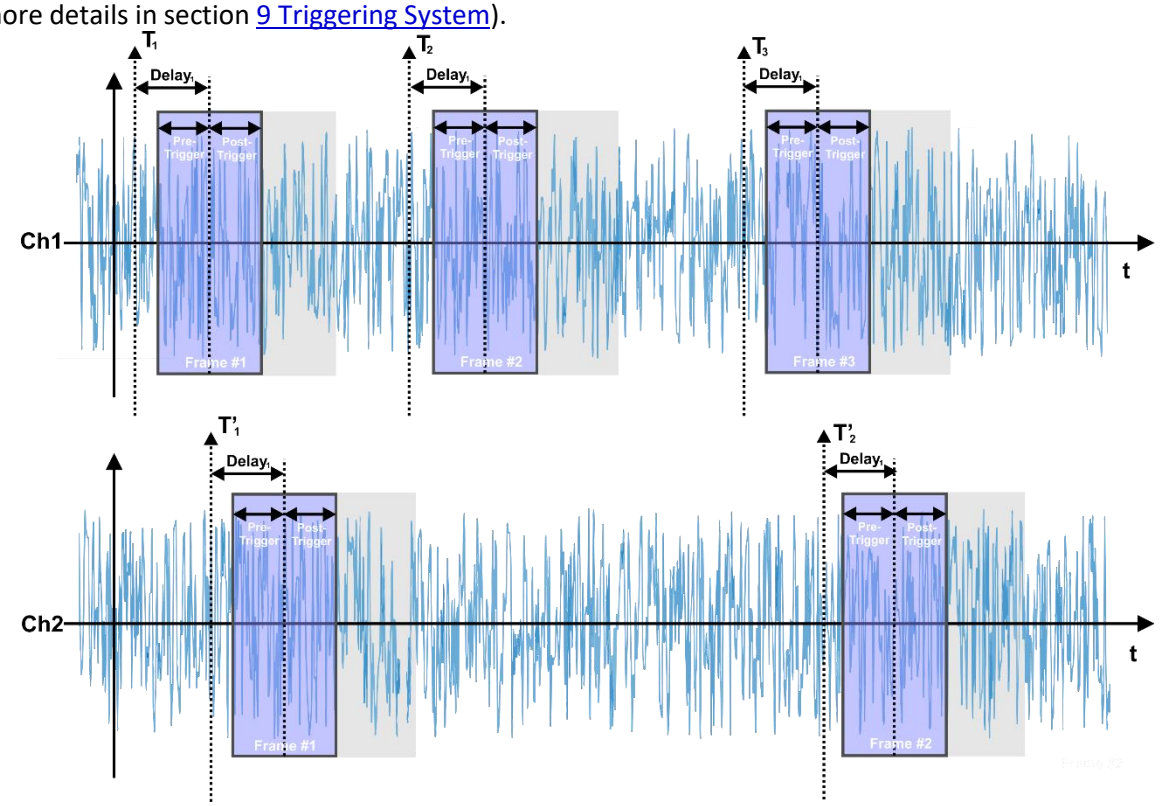

Figure 10.9 Independent Acquisition

Waveform acquisition for both channels can be based in a common or different trigger event. However, the digitizer will acquire a frame only when the trigger condition is armed for that particular channel. When the trigger event is different for each channel, the way frames are acquired depends only on the conditions for each channel (Figure 10.10). When both channels use the same trigger condition, as the trigger position and delay is always the same for both channels, captures will consist in fully aligned frames for both channels. When the trigger source is not the same for both channels, each acquisition is carried out according to each trigger event so

acquisitions will not be aligned and the evolution of a multi-frame acquisition will be asynchronous, so the status for each channel should be checked independently.

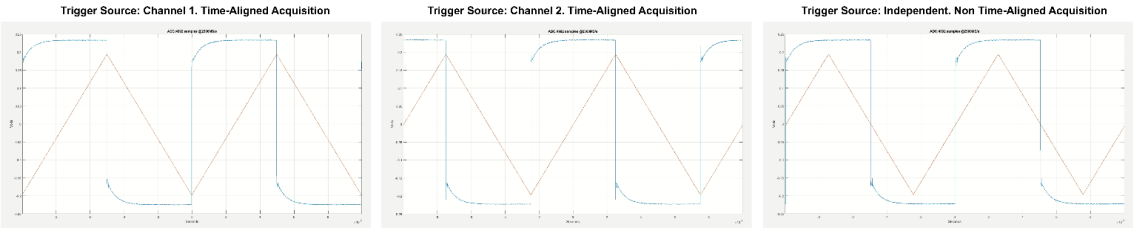

Figure 10.10 Two-Channel Self-Triggered Acquisitions with Trigger Source from Ch1 (Left), Ch2 (Middle), and Independent (Right)

When using the EXT trigger source, the status of the trigger signal can be part of the acquisition by activating the Marker Mode. In this mode, the least-significant bit (LSB) for each sample in the acquisition is a marker holding this information. As a result, one bit of the ADC resolution is lost. While in the marker mode, the LSB can signal the position of the closest sample to the trigger event. As previously mentioned, acquisitions are made in chunks of 48 samples (96 samples in the dual mode) and the trigger event can be aligned with any of the samples in a given chunk. Therefore, the resolution for the trigger position is limited by the chunk size. Using the marker mode, trigger position resolution is reduced to 1 sample period, see figure below.

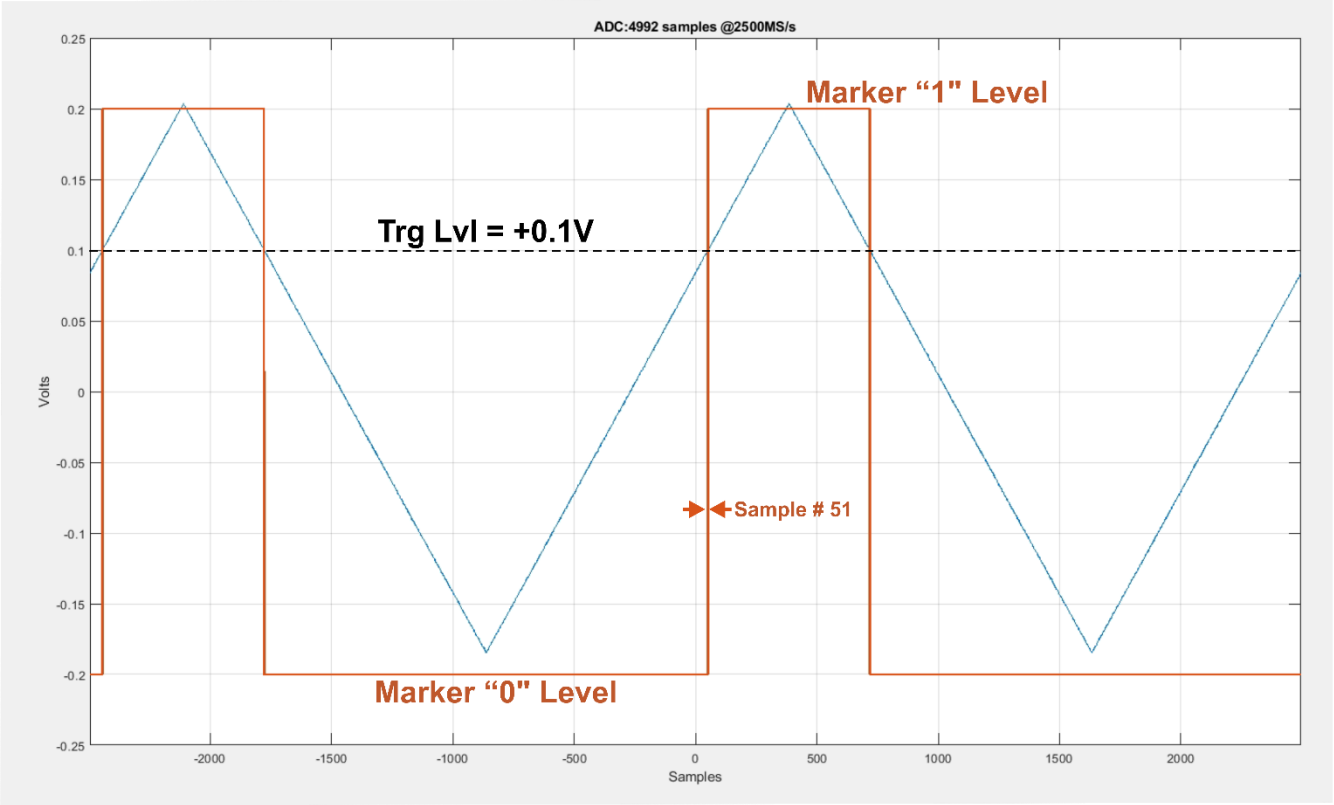

Figure 10.11 Marker Mode

Sample rate is controlled by the sampling clock. Sampling clock can come from three different sources:

- Digitizer: The digitizer block incorporates its own sampling clock synthesizer. This synthesizer is locked to the same internal or external reference as the AWG internal sampling clock.
- AWG: The sampling clock is derived directly from the AWG sampling clock so sampling for both sections is synchronous. As AWG sampling clock can reach up to 9GHz, and the maximum sampling clock in the dual channel mode is 2.7GHz, beyond this sampling frequency for the AWG section, synchronous sampling is only possible using interpolated modes in the AWG section (Table 4.2 Waveform Sampling Rate Range vs. DAC Sampling Rate as a Function of the Interpolation Factor) or by setting up the ADC sampling rate to be a x2, x4, or x8 submultiple of the AWG's. This setting is especially useful when the signals being acquired are somehow related to the signals being generated by the AWG section.
- External: This is the external Sclk input (SCLK IN) on the Proteus front panel (see Figure 10.14 Proteus).

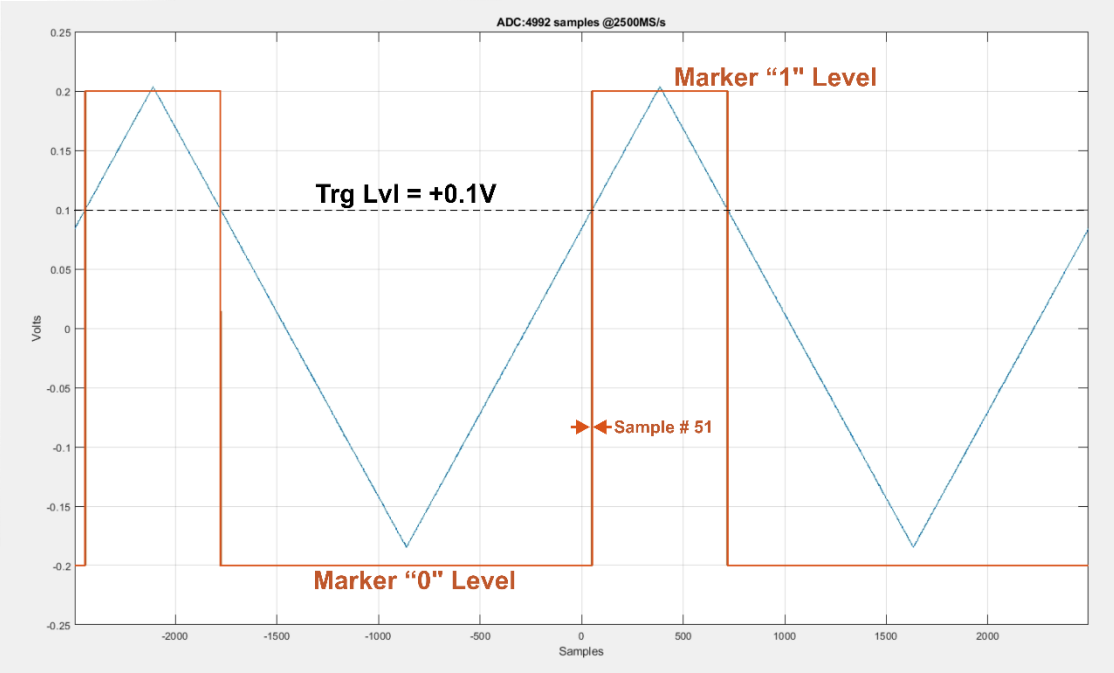

Figure 10.12 Trigger Signal Applied to Ext Trigger Input and Ch1. The Red Trace Shows the Contents of the LSB of the Acquired Waveform in the Marker Mode and the Actual Position of the Trigger Event

The digitizer can perform additional functions besides the pure acquisition of waveforms in frames. These are the available functions:

- Averaging: Linear averaging is a very effective way to remove noise of repetitive signals and also to extract repeating patterns embedded in non-repeating signals. It can also be used to improve vertical resolution, always for repetitive waveforms. Typically, averaging requires acquiring multiple time-aligned waveforms, add them together, and divide by the number of waveforms. Although average processing is fairly simple, collecting, transferring and calculating the average waveform may be memory and time consuming. The automatic averaging function in the Proteus ADC can carry out all this processing in real time without the need to accumulate multiple waveforms so a very large saving in terms of time and memory is accomplished. The internal averaging function is limited to capture frames with 10224 samples or lower and the average can be calculated for up to 16M acquisitions per frame. As the sample resolution increases with the number of averages (ΔRes = $\log_2$(num_of_avg)), waveform data from average frames consists in unsigned 32-bit integers. Only the 28 LSBs are actually used. To properly scale these unsigned 32-bit number to the 12-bit ADC normalized range (0-4095), the following steps must be applied:
    1. Subtract 227 from each sample value so s'(n) = s(n) - 227. And convert the number to double-precision floating point numbers
    2. Calculate the number of bits resulting from the averaging process using the DRes = floor(log2(num_of_avg)) expression.
    3. Calculate s''(n) = s'(n) / num_of_avgs
    4. If DRes > 16, the s''(n) must be properly scaled to account for the truncated bits so the final s'''(n) = 2048 + s´´(n) * 2(DRes -16). Otherwise, s'''(n) = 2048 + s''(n). The resulting s''' floating point values will be scaled between 0 and 4095
- Loopback: It transfers, in real-time, the acquired signal from one of the digitizer channels to any of the AWG channels. To activate this function, sample rate for both sections must be synchronous (see sampling clock source above). The loopback functionality allows for the selection of the source channel in the digitizer and the target channel in the AWG sections. It also allows for adding a time delay and phase offset of the captured signal. The delay between the input and the output can accept values 8 to 2047 where each value corresponds to 16*DAC_SCLK_Period.
- Pulse Counter: There is one pulse counter per digitizer channel. It counts trigger events without the need to capture any waveform. It can be used to count external or internal events (including those generated by the AWG section) continuously or during a user-defined time-gate. Pulse counter status is one of the fields in the status string (see above description) and their values can be read at any time or after the time gate has expired.

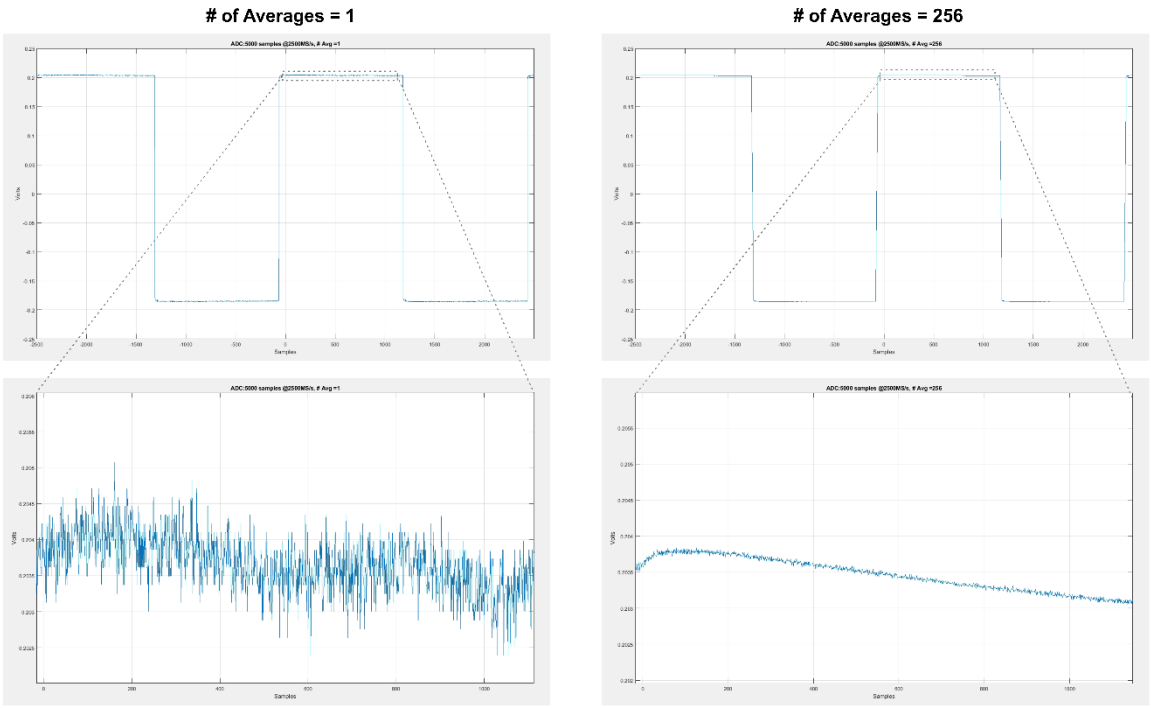

Figure 10.13 Averaged Acquisitions of Repetitive Waveforms (Right) Results in Lower Noise and Higher Resolution Acquired Waveform Respect to Non-Averaged Waveforms (Left)

10.5 Trigger Modes

Figure 10.14 Proteus P9484M-AWT Front Panel

Trigger conditions may be defined independently for each channel. It is possible to trigger both channels with the same trigger event as trigger conditions may be set to the same parameters. To find out how trigger events handle frame acquisition and how acquisitions are aligned to these trigger events, refer to 10.4 Acquisition Modes.

Trigger events may be internal or external. Internal triggers may be related to conditions met by the signals being acquired or by conditions generated internally by the AWT. External triggers are those generated by the TRIG IN input.

The trigger source can be selected among the following choices:

- CPU: This is a software trigger without any correlation to internal or external events. It is activated by the ***:TRIGger:IMMediate*** or the ****TRG*** SCPI commands.
- EXT: External trigger comes from the external trigger input in the front panel (TRIG IN, see above figure).
- CH1/CH2: Any of the input channels in the digitizer. Both channels can be assigned as the trigger source for any of them.
- TASK1/TASK2/TASK3/TASK4: Trigger comes from the task sequencer for a particular channel (1 to 4) in the AWG section of the Proteus AWT (see 6.3 Task Table Parameters). A fixed delay can be added to delay the acquisition respect to the task generated event end condition.

- MR1/MR2: Rise of the marker bit in a given digitizer channel (see Figure 10.11 Marker Mode).
- MF1/MF2: Fall of the marker bit in a given digitizer channel (see Figure 10.11 Marker Mode).

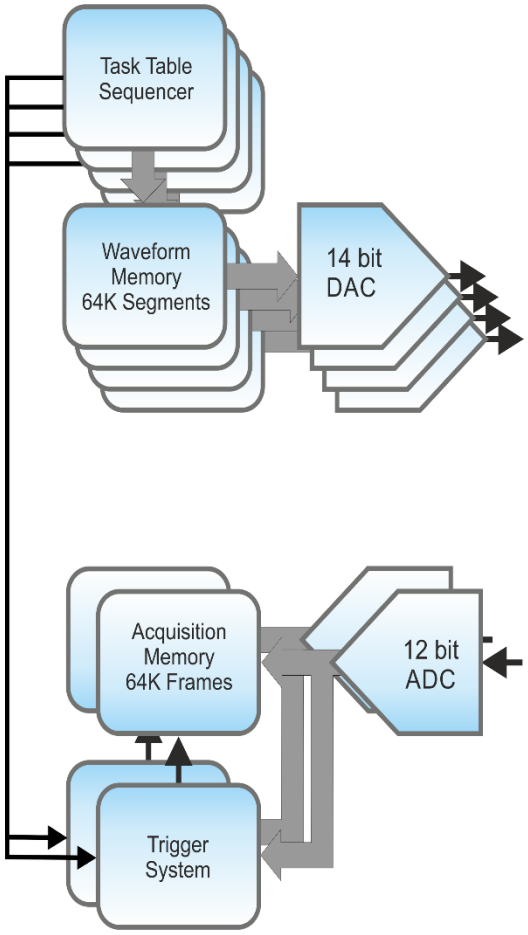

Figure 10.15 Task Trigger

Defining the trigger source is just the first step to define the trigger condition and functionality. For some trigger events it is possible to define the level and edge (positive or negative) validating the trigger event. This includes the SELF trigger mode (the input signal level is used for trigger) or the EXT trigger (the external trigger input in the front panel). For this category of trigger events, setting level and edge is enough if the EDGE mode is set. However, more complex trigger conditions may be set by acting according to timing parameters. Trigger types are listed below:

- EDGE: Just crossing the threshold in the corresponding edge (positive/negative) will result in a valid trigger event. For self-trigger, trigger level range depends on the selected input range: For low range trigger level goes from -125mV to +125mV, -200mV to +200mV for the medium range, and -250mV to +250mV for the high range.
- GATE: The acquisition is controlled by the gate conditions applied to the External Trigger Input. Gate can be defined based in different voltage thresholds for the beginning and the end of the gate.

- WINDOW GATE: The trigger condition is valid when a given level condition is true for a time greater or shorter than a given window width. Edge and thresholds can be set independently for the conditions starting and finishing the window. The trigger event occurs at the end of the window.

10.6 Frame Header

Each acquired frame is associated to a header where some relevant information about the acquisition is stored and it can be retrieved, when necessary, along with the waveform data or independently. The header consists of a 88 bytes long bitfield. The first 5 fields are associated to the frame itself while the rest is associated to the DSP functionality (refer to the Proteus Programming Manual section "Digital Signal Processing Commands"). The contents of the fields associated to the frame are the following:

Table 10.1 First 5 Frame Header Fields

#	Name	Bits	Description
1	Trigger Location in the Frame	31:0	This information is aligned with the pre-trigger functionality.
2	Gate Mode Last Address	63:32	Associated with the Gate Mode.
3	Min Vpp	95:64	Minimum sample value within the frame.
4	Max Vpp	127:96	Maximum sample value within the frame.
5	Timestamp	191:128	Timestamp for the trigger event associated to the frame.

Detailed Description

Field #1: Trigger Location in the Frame

The pre-trigger settings for a given acquisition of any number of frames is defined by the user as explained in the previous paragraph of this section of the manual. Knowing this information is important so the right location of the trigger event can be recovered from the acquisition and the absolute timing respect to the trigger event can be established. This field is 32 bits long and must interpreted as an unsigned 32 bits integer. The size of the field can accommodate even the longest possible value set by the user for the pre-trigger parameters and it is expressed in samples.

Field #2: Gate Mode Last Address

Sample number for the last sample within the interval defined by the gate (see GATE trigger above).

Field #3: Minimum Sample Value Within the Frame

This field is 32 bits long although only the 12 LSBs are actually meaningful. It contains the minimum level obtained from the ADC for the current frame. It is expressed in digitizer levels (0-4095). Actual voltage level must be calculated from the range and offset settings.

Field #4: Maximum Sample Value Within the Frame

This field is 32 bits long although only the 12 LSBs are actually meaningful. It contains the maximum level obtained from the ADC for the current frame. It is expressed in digitizer levels (0-4095). Actual voltage level must be calculated from the range and offset settings. Subtracting the contents of field #3 from field #4, the Amplitude Peak-to-Peak can be obtained for any frame.

Field #5: Timestamp

The timestamp field contains the absolute time from the time reference for the trigger event for the current frame regardless of the actual position of the closest sample to the trigger event within the frame. The 64-bit long field must be interpreted as unsigned 64-bit integer. Time is measured in sample clock cycles so the absolute time (AT) measured in seconds can be calculated from the timestamp (TS) using the following formula:

```
AT = TS / SR
```

Where SR = Digitizer Sampling Rate.
Although, the timestamp value is expressed in sampling clock cycles, the resolution of the stamp is 20 sampling clock cycles. It is important to understand that timestamps reflect the absolute timing for the trigger event for the current frame. Any trigger event not resulting in a frame acquisition (i.e. because some valid trigger condition occurs while pre-trigger information being filled or before trigger is re-armed immediately after some frame acquisition ends due to the hold-off time.
Timestamps can be used as a timing measurement function so the precise timing between trigger events can be acquired without acquiring, uploading, and processing waveform data so it can work at a much higher speed than methods based in waveform analysis.

10.7 DDC Operation

Each digitizer channel can feed a DDC (Digital Down-Converter) block. The DDC may be used for different purposes:

- Converting a bandwidth-limited real signal to its baseband equivalent complex (I/Q) signal.
- Selecting any portion of the spectrum for storage and/or further analysis.
- Waveform data reduction as decimation can be applied.
- Increase of ADC effective resolution as a consequence of processing gain.
- Signal demodulation.

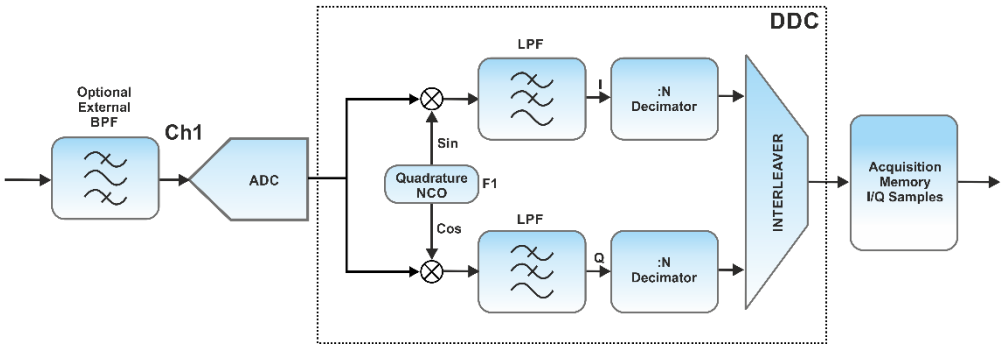

Figure 10.16 Digital Down-Converter (DDC)

The block diagram of the DDC is shown in the above figure. The digitized waveform is fed to two multipliers where the output of a quadrature NCO is also applied. The output of the multipliers goes through digital low-pass filters (LPF), and finally the waveforms are decimated by an integer factor (decimation factor, 4X, and 16X user-selectable). The cutoff frequency of the LPF is a function of the sample rate and the decimation factor (DF) so both the I and Q waveforms are aliasing-free. The usable BW of the DDC (or analysis BW) can be calculated using the following expression:

```
UBW = 0.85 x Sclk / DF
```

The above expression results in an analysis bandwidth of up to 1.15GHz at 2.7GS/s and 2x decimation factor. The real (I) and imaginary (Q) waveform samples are interleaved and stored in the waveform memory. Frame size must be defined in real samples so the size must be set to twice the number of the desired number of complex samples.

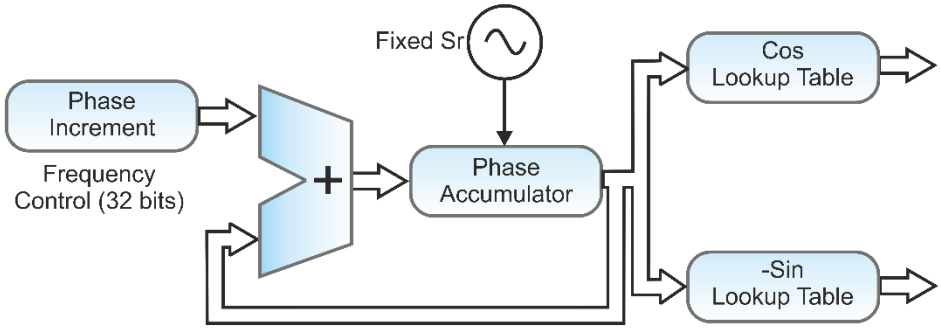

Figure 10.17 NCO Block Diagram

Tuning the frequency for the DDC block is established by the frequency setting for the NCO (refer to the above figure). The NCO in the digitizer produces two sinewaves with 90° degrees phase (quadrature carriers). The NCO is based in the Direct Digital Synthesis (or DDS) architecture so the frequency can change instantaneously. In a DDS, the frequency is controlled by the contents of a frequency control register. In the Proteus digitizer the frequency control register of the NCO is 32-bit wide. This means that after setting the central frequency for the acquisition, the actual frequency is the closest one to one of the following:

$$FNCO = Sclk \times 2^{-32} \times N$$

Where N is an integer in the 0 to 232-1 range.
The above expression results in a frequency resolution of 0.629Hz for Sclk = 2.7GS/s. The DDC can be used in both the DUAL and the SINGLE mode. However, it is usable at sample rates up to 2.7GS/s no matter the mode. In the single mode, though, both NCOs (one per channel) can be applied to CH1 if the sampling rate is set to 2.7GS/s or lower (see Figure 10.3 Digitizer Section Block Diagram for SINGLE Mode). This is the only real motivation to use the SINGLE mode for sample rates equal or lower than 2.7GS/s. This allows for the down-conversion or demodulation of two different bands (that may overlap) using the same decimation factor. In this situation, frame size must be defined in real samples so the size must be set to four times the number of the desired number of complex samples for each of the baseband waveforms.
The DDC main area of application is RF signal acquisition. It can be combined with down-conversion by under-sampling to the first Nyquist Zone as shown in Figure 10.2 Capturing Signals Beyond 1st Nyquist Band. Special care must be taken in order to avoid signal interference and reduce noise. These are the steps to follow to achieve this objective:

- Apply one or more external, high quality band-pass filter and amplifier to select the wanted signals, remove unwanted signals from the front end, and adapt the amplitude to optimize the ADC's dynamic range being applied to the wanted signals.
- Make sure the wanted signals are all located within the boundaries of one of the usable Nyquist Zones of the ADC. This can be accomplished by setting a convenient Sclk.

- When wanted signals are located in more than one NZ, sample rate must be set in a way the images in the first NZ do not overlap in the bands under the band set by the analysis bandwidth being applied (see below figure).

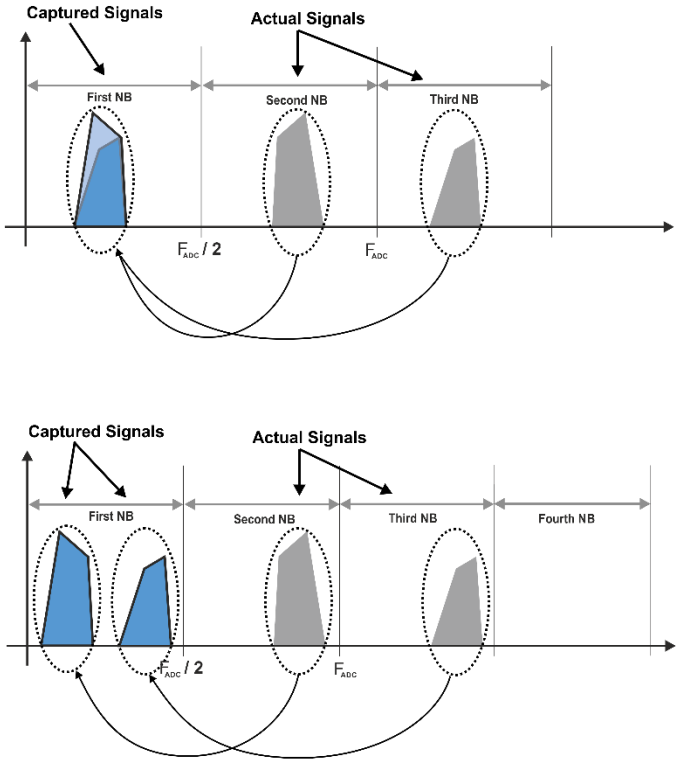

Figure 10.18 DDC RF Signals Over Multiple NZ

If any down-converted RF signal is located in an even numbered NZ, the spectrum of the complex baseband signal will be inverted. There are two methods to remove this effect. The first method consists in inverting one of the components of the baseband complex signal (either I or Q). The second one consists in setting the NCO frequency to the image frequency of the carrier in the second NZ (F_{NCO2} = Sclk – F_{NCO1}).

The decimation process results in a processing gain regarding the effective bits at the output of the DDC. An additional bit is obtained for every 4x decimation. This results in two additional bits for the 16x decimation factor. Samples at the output of the DDC use 15-bit resolution, so the two additional bits can be accommodated while avoiding any calculation noise coming from rounding of the LSB. Samples are stored as 24-bits words, so additional processing gain can be accommodated while calculation noise resulting for additional digital signal processing does not reduce effective resolution.

As complex down-converted baseband signals are stored as interleaved IQ pairs, waveforms read from the Proteus digitizer must be de-interleaved by the control SW. In the SINGLE mode, when both DDCs are applied to the input signal, waveform data is returned as double interleaved quadruplets (I1, Q1, I2, Q2) so a double de-interleaving process must be carried on.

NCO's frequency and phase can be coherent over multiple channels. Selecting the right frequencies, the NCOs in the digitizer can also be coherent with the NCOs in the DUCs in the AWG section of Proteus. Relative phase can also be set deterministically so coherence can be kept as long as desired

over multiple generation and acquisition channels and obtain repeatable phase settings for multiple tests.

Coherent Operation of The DUC and the DDC

Some application may require the coherent IQ demodulation of some waveform originally generated using the DUC in the AWG section of the same Proteus unit. In this way, the phase and/or frequency shifts introduced by the device/system under test could be obtained. This functionality also eases the processing of the acquired RF signal as there is no need to recover the carrier at the receiver side. The flexibility provided by Proteus, where all the generation and acquisition settings for the AWG and Digitizer sections can be set independently (although they may be using the same frequency reference), do not result in the automatic coherent operation of the DUC and the DDC even if they are set to the same FNCO.

Proteus allows for the coherent operation of the DUC and the DDC if some conditions are met:

- Sclk for the DAC is a x1, X2, X4, or x8 multiple of that of the ADC. When this condition is met, and the ADC is set in the Coherent Mode (through the ***:DIGitizer:DDC:CLKSource AWG*** command), the sampling clock source for the digitizer is the sampling clock from the AWG divide by the multiplication factor.
- The F_{NCO} (Numerically Controlled Oscillator Frequency) for both the AWG and the ADC is set to the same frequency. This implies that DUC/DDC coherent operation does not work beyond the ADC's Sample Rate frequency.

When the above conditions are met, the NCOs in the DUC and the DDC will operate in a coherent manner for any period of time. In addition, the phase between both blocks will be deterministic so the DUC to the DDC phase can be adjusted using the commands associated to initial phase control for the NCOs.
It is important to realize some of the implications of coherent operation of the DUC and DDC. First, the size of the phase accumulator in the NCO (see Figure 10.17) for the DUC (48 bits) and the DDC (32 bits). This means that even setting the same frequency for both blocks, the actual frequency being generated by both NCOs can be different due to the rounding involved in the calculation of the frequency control word. In order to avoid this, when operating in the Coherent Mode, the frequency control word of the NCO in the DUC is automatically calculated with a reduced resolution. At the same time, in order to get the same frequencies out of the NCOs, the frequency control word for the DDC must be set in a way it compensates the 1x, 2x, 4x, or 8x ratio (ADR) respect to the AWG sampling rate. To meet that condition, the frequency control word of the DUC (48 bits) is calculated setting some LSBs to 0. The number of active most significant bits (ABDUC) in the DUC can be calculated using the following expression:

$$ABDUC = 32 + \log_2(ADR)$$

The 48-ABDUC least significant bits are set to zero. The frequency control word for the NCO in the DDC is automatically obtained by multiplying the frequency control word for the DUC by the AWG/Digitizer sampling rate ratio (ADR) and then extracting the 32 MSBs. This way to operate results in the reduction of the frequency resolution (FR) of both the DUC and DDC (the same by definition as they operate coherently):

$$FR = SRAWG / 2^{ABDUC}$$

The maximum sampling rate of the AWG may be higher than the one of the Digitizer in Proteus. This means that beyond the maximum ADC's sampling rate, the only way to operate the DUC and the

DDC coherently is by using a x2, x4 o x8 ratio between the DUC and the DDC. Under non-coherent conditions, the FNCO for the DUC and DDC can be set between 0Hz and the sample rate. This would result in the impossibility to work in a coherent, deterministic way when the target carrier frequency is located beyond the second Nyquist Zone of the digitizer, although this signal can be acquired using under-sampling by the ADC.

11 Remote Control

11.1 Introduction

The Proteus module platform must be used in conjunction with a host computer. There are three ways to program the device, the first being low-level programming of each individual parameter, using SCPI commands. The second alternative is to use WDS (Wave Design Studio) for high-level programming. WDS is a software package supplied with the device that enables full control and programming via a user-friendly graphical user interface. The third alternative is using application specific drivers, such IVI (Interchangeable Virtual Instrument) or LabVIEW drivers.

11.2 Wave Design Studio

The WDS is the latest in instrument control and signal creation software. It enables full remote control of Tabor's waveform generators and simplifies the creation of complex signals. With a modern and intuitive graphical user interface WDS offers easy access and control of all the instruments features and capabilities. In addition to the standard waveform creation tools, WDS offers waveform creation add-ons for radar, and future microwave, RF and general-purpose applications. Refer to Wave Design Studio (WDS) User Manual that can be downloaded from www.taborelec.com/downloads.

11.3 SCPI Programming

SCPI (Standard Commands for Programmable Instruments) is an ASCII-based instrument command language designed for test and measurement instruments. SCPI commands are based on a hierarchical structure, known as a tree system. In this system, associated commands are grouped together under a common node or root, consequently forming subsystems.
For a detailed explanation of how to program the instrument through SCPI commands please refer to the "Proteus Programming Manual".

Tip
Use the WDS command editor and log window (Menu > Options) to learn how to program the unit with SCPI commands. All SCPI commands are logged in the log window and the command editor enables sending specific SCPI commands to the instrument.

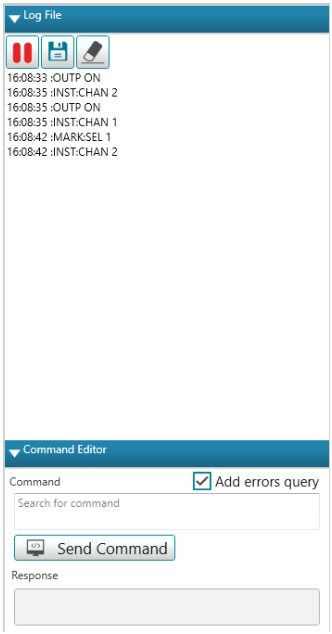

Figure 11.1 WDS Log Window and Command Editor

11.4 IVI Driver Programming

An alternative method for programming is using the IVI instrument driver. The IVI driver is an instrument driver specified by the IVI (Interchangeable Virtual Instrumentation) foundation, that follows a set of software routines that simplify the programming of test and measurement instruments. The IVI driver for the Proteus instrument is available on the CD supplied with your Proteus device or for download from the Tabor website.

12 Proteus Module Specifications

Note

The specifications are given for all the Proteus series models, i.e., Module (M), Benchtop (B), and Desktop (D).

12.1 Channels Characteristics

Table 12.1 Channels Characteristics Specifications

Parameter	P908xy[1]	P258xy[1]	P128xy[1]	P948xy[1]
FORM FACTOR[1]	M/B/D	M/B/D	M/B/D	M/B/D
NUMBER OF CHANNELS	M=2, B=2/4/6, D=2/4/6	M=2/4, B=2/4/8/12, D=2/4/8/12	M=2/4, B=2/4/8/12, D=2/4/8/12	M=2/4, B=2/4/8/12, D=2/4/8/12
INITIAL SKEW				
BETWEEN CHANNELS	<50ps typ., 1 SCLK max.			
BETWEEN MODULES	<100ps typ., 1 SCLK or 300ps max.			
FINE DELAY				
RANGE	0 to 3ns			
RESOLUTION	5ps			
ACCURACY	±5ps			
COARSE DELAY				
RANGE	0 to wavelength			
RESOLUTION	1 sample point			

[1] x = Number of channels, y=M/B/D=Module/Benchtop/Desktop.

12.2 Arbitrary Mode

Table 12.2 Arbitrary Mode Specifications

Parameter	P908xy	P258xy	P128xy	P948xy
MAX. SAMPLE RATE	9GS/s	2.5GS/s	1.25GS/s	9GS/s
RESOLUTION	8-bit	16-bit		
MAX. MEMORY SIZE	Up to 16GS	Up to 8GS		
NUMBER OF SEGMENTS	64k			
MINIMUM SEGMENT LENGTH NORMAL FAST SEGMENT	2048 points 224 points	1024 points 64 points		
WAVEFORM GRANULARITY STANDARD OPTIONAL	64 points 32 points	32 points 16 points	32 points 16 points	32 points 16 points

12.3 Task Mode

Table 12.3 Task Mode Specifications

Parameter	Description
TASK TABLE LENGTH	64K tasks per channel
TASK LOOPS	1M
SEQUENCE	A sequence is defined as a continuous and looped series of tasks

Parameter	Description
MAX. NUMBER OF SEQUENCES	32k sequences
SEQUENCE LOOPS	1M
SCENARIO	A scenario is defined as a continuous series of tasks/sequences
MAX. NUMBER OF SCENARIOS	1k scenarios

12.4 Streaming (STM Option)

Table 12.4 Streaming (STM Option) Specifications

Parameter	Description
MAX. STREAM RATE	Up to 6GS/s
MINIMUM PC REQUIREMENTS	
CPU	i7
MEMORY	32GB
OPERATING SYSTEM	Windows 10
SOURCE	PXI Express Bus

12.5 Signal Purity

Table 12.5 Signal Purity Specifications

Parameter	DC OUTPUT	DIRECT OUTPUT
HARMONIC DISTORTION [2]		
fout = 10 MHz - 200 MHz, Measured @ DC to 2 GHz	<-70 dBc (typ.)	<-70 dBc (typ.)
fout = 200 MHz - 1.5 GHz, Measured @ DC to 4.5 GHz	<-60 dBc (typ.)	<-60 dBc (typ.)
fout = 1.5 GHz - 4.5 GHz, Measured @ DC to 4.5 GHz	<-50 dBc (typ.)	<-50 dBc (typ.)
SFDR [3]		
fout = 10 MHz…500 MHz, Measured @ DC to 1.5 GHz	-80 dBc (typ.)	<-85 dBc (typ.)
fout = 500 MHz…4.5 GHz , Measured @ DC to 4.5 GHz	-70 dBc (typ.)	<-75 dBc (typ.)
PHASE NOISE (@10kHz offset)		
fout = 140.625MHz	-134 dBc/Hz	
fout = 280.25MHz	-128 dBc/Hz	
fout = 562.5MHz	-122 dBc/Hz	
fout = 1.125GHz	-116 dBc/Hz	
fout = 2.25GHz	-110 dBc/Hz	
fout = 4.5GHz	-104 dBc/Hz	

[2] SCLK=Max sample rate, amplitude = 400 mVpp, direct mode, measured using balun.
[3] SCLK=Max sample rate, amplitude = 400 mVpp, excluding SCLK/2-fout, measured using a balun.

12.6 DC Output

Table 12.6 DC Output Specifications

Parameter	Description
OUTPUT TYPE	Single-ended or differential, DC-coupled
IMPEDANCE	50Ω (nom)
AMPLITUDE	50 mVp-p to 1.3 Vp-p
AMPLITUDE RESOLUTION	1mV
DC AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)
VOLTAGE WINDOW	±1.15V
DC OFFSET	±0.5V
OFFSET RESOLUTION	10mV
DC OFFSET ACCURACY	±(3% of setting ±15 mV)
SKEW BETWEEN NORMAL AND COMPLEMENT OUTPUTS	0ps
RISE/FALL TIME (20% TO 80%)	< 130 ps (typ.)
INSTANTANEOUS BANDWIDTH P128xy | P258xy | P908xy | P948xy	 625MHz | 1.25GHz | 4.5GHz | 4.5GHz
MAX. USABLE FREQUENCY P128xy | P258xy | P908xy | P948xy	1st/2nd Nyquist 1.25GHz | 2.5GHz | 4.5GHz | 4.5GHz
JITTER (PEAK-PEAK)	<15 ps (typ.)
OVERSHOOT	<5% (typ.)
CONNECTOR	SMA

12.7 Direct Output

Direct output is standard for P9482M/P9484M and optional for all other Proteus models.

Table 12.7 Direct Output Specifications

Parameter	Description
OUTPUT TYPE	Single-ended or differential, AC coupled
IMPEDANCE	50Ω (nom)
AMPLITUDE SINGLE-ENDED DIFFERENTIAL	 1mVpp to 550mVpp, single-ended into 50Ω 1mV to 1.1Vpp
AMPLITUDE RESOLUTION	1mV
AMPLITUDE ACCURACY	±(3% of amplitude ±2 mV)
RISE/FALL TIME (20% TO 80%)	< 60 ps (typ.)
INSTANTANEOUS BANDWIDTH P128xy | P258xy | P908xy | P948xy	 625MHz | 1.25GHz | 4.5GHz
MAX. USABLE FREQUENCY P128xy | P258xy | P908xy | P948xy	3rd Nyquist 1.25GHz | 2.5GHz | 10GHz | 10GHz
SKEW BETWEEN NORMAL AND COMPLEMENT OUTPUTS	0 ps
JITTER (PEAK-PEAK)	<15 ps (typ.)
CONNECTOR	SMA

12.8 Sample Clock Output

Table 12.8 Sample Clock Output Specifications

Parameter	Description
SOURCE	Selectable, internal synthesizer or sample clock input
FREQUENCY RANGE	SCLK range
OUTPUT AMPLITUDE	0.5V to 1V depending on SCLK
IMPEDANCE	50Ω (nom.), AC coupled
CONNECTOR	SMA

12.9 Sync Clock Output

Table 12.9 Sync Clock Output Specifications

Parameter	Description
AMPLITUDE	500mVpp, typ.
FREQUENCY P908xy P128xy, P258xy P948xy	 SCLK/32 SCLK/8 SCLK/8 (standard), SCLK/32 (x1 mode)
WAVEFORM	Square
RISE/FALL TIME (20% TO 80%)	<150ps
IMPEDANCE	LVCMOS
CONNECTOR	SMP

12.10 Marker Outputs

Table 12.10 Marker Outputs Specifications

Parameter	Description
NUMBER OF MARKERS	Refer to ordering information
OUTPUT TYPE	Single ended
OUTPUT IMPEDANCE	50Ω (nom.)
AMPLITUDE	
VOLTAGE WINDOW	±1.15V
LEVEL	32mVpp to 1.2Vpp (32 discrete levels)
RESOLUTION	10mVpp
ACCURACY	±7%
OFFSET	
RANGE	±0.5V
RESOLUTION	10mV
ACCURACY	±(3% of setting ±15 mV)
RISE/FALL TIME (20% TO 80%)	<200ps
MARKER LENGTH	0 - waveform length
RESOLUTION P128xy, P258xy P9082y P948xy	 2 pts 8 pts 2 pts (standard) 8 pts (x1 mode)
MARKER DELAY	
COARSE DELAY	
RANGE	0 to 2048 points
RESOLUTION P128xy, P258xy P9082y	8 points

Parameter	Description
P948xy	32 points 8 pts (standard), 32 pts (x1 mode)
FINE DELAY	
RANGE	0 to 1.2ns
RESOLUTION	1ps
ACCURACY	15ps
CONNECTOR	SMP

12.11 Reference Clock Output

Table 12.11 Reference Clock Output Specifications

Parameter	Description
SOURCE	Internal TCXO
WAVEFORM	Square
FREQUENCY	100MHz or REF IN
STABILITY	+/- 2.5 PPM
AGING	+/- 1 PPM @ +25°C (per year)
CONNECTOR	SMP

12.12 Reference Clock Input

Table 12.12 Reference Clock Input Specifications

Parameter	Description
INPUT FREQUENCIES	10MHz / 100MHz selectable
LOCK RANGE	± 1MHz
INPUT LEVEL	0.6 Vp-p to 1.7 Vp-p
IMPEDANCE	50Ω, AC coupled (nom.)
CONNECTOR	SMP

12.13 Sample Clock Input

Table 12.13 Sample Clock Input Specifications

Parameter	Description
FREQUENCY RANGE	SCLK Range
INPUT LEVEL RANGE	0.4Vpp to 1.2Vpp
DAMAGE LEVEL	<-0.5V or >1.5V
INPUT IMPEDANCE	50Ω nom., AC coupled
CONNECTOR	SMA

12.14 Trigger Inputs

Table 12.14 Trigger Inputs Specifications

Parameter	Description
RANGE	–5V to +5V
THRESHOLD	±5V
RANGE	–5V to +5V
RESOLUTION	100mV
SENSITIVITY	200mV
JITTER STANDARD P128xy, P258xy,P908xy P948xy LOW TRIGGER JITTER OPT.	 8 SCLK periods 32 SCLK periods 8 SCLK periods (standard), 32 SCLK periods (x1 mode) SQRT(SCLK period^2 + 150e-12^2)
LATENCY / SYSTEM DELAY P128xy, P258xy, P948xy STANDARD P908xy, P948xy x1 MODE	 <900 SCLK periods <2700 SCLK periods
POLARITY	Positive or negative
SOURCE	Selectable between channels
INPUT IMPEDANCE	10kΩ or 50Ω (nom.), DC coupled, factory configured
MAX TOGGLE FREQUENCY	10MHz (50MHz optional)
MINIMUM PULSE WIDTH	50ns (5ns optional)
CONNECTOR	SMP

12.15 Fast Segment Dynamic Control Input (Optional)

Table 12.15 Fast Segment Dynamic Control Input (Optional) Specifications

Parameter	Description
INPUT SIGNALS	Data 10bit, channel select 2 bit, valid 1 bit
SEGMENTS / SEQUENCES	1024 (128 fast)
DATA RATE	35MHz
MINIMUM LATENCY (Dynamic control input to direct out)	
FAST SEGMENT	<250ns
NORMAL SEGMENT	<1µs
INPUT LEVEL	LVTTL
CONNECTOR	MDR

12.16 Digitizer Characteristics (AWT Option)

Table 12.16 Digitizer Characteristics (AWT Option) Specifications

Parameter	Description
NUMBER OF CHANNELS	1 or 2
INPUT VOLTAGE RANGE	500 mVpp (full scale)
INPUT VOLTAGE OFFSET	-2V to +2V
INPUT FREQUENCY RANGE	9GHz
RESOLUTION	12 bits
ACQUISITION MEMORY	Up to max. arbitrary memory
SAMPLE CLOCK SOURCES	Internal or external
INTERNAL CLOCK SOURCE	Internal, external reference
MAX SAMPLING RATE	5.4GS/s in single channel mode 2.7Gs/s in dual channel mode
MIN SAMPLING RATE	800Ms/s
CLOCK ACCURACY	<2 ppm

Parameter	Description
IMPEDANCE	50Ω
COUPLING	DC or AC (factory configured)
TRIGGER SYSTEM	
TRIGGER MODES	Positive, negative edge
TRIGGER SOURCES	External, software, channel
COUPLING	DC
IMPEDANCE	50Ω (nominal)
LEVEL RANGE	>± 2.5 V (nominal)
FREQUENCY RANGE	DC to 65MHz
CONNECTOR	SMA

12.17 FPGA Programming

Table 12.17 FPGA Programming Specifications

Parameter	Description
FPGA TYPE	Xilinx Kintex UltraScale XCKU060 upgradeable to XCKU115
MODES	
STANDARD	Tabor standard built-In functionality
DECISION BLOCKS	Built-in library of mathematical functions, modulation & digital filters
SHELL	Open core providing all interfaces and configuration path to the user

12.18 Digital Upconverter

Table 12.18 Digital Upconverter Specifications

Parameter	Description		
MODES P258xy, P948xy ALL OTHERS MODELS	 NCO / interpolation / IQ modulation NCO only		
SAMPLING RATE	1GS/s to max. sample rate		
CARRIER FREQUENCY			
RANGE	0 to 40% of sampling rate		
RESOLUTION	48 bit		
PHASE RANGE	0 to 360°		
PHASE RESOLUTION	16 bit		
INTERPOLATION FACTORS	x2, x4, x8		
IQ FORMAT P258xy	x2 mode		
IQ PAIR PER CHANNEL	1		
MAX INPUT RATE	1,250MS/s		
NUMBER OF CHANNELS	2		
IQ FORMAT P948xy	x2 mode	x4 mode	x8 mode
IQ PAIR PER CHANNEL	1	1	1 or 2
MAX INPUT RATE	2,500MS/s	2,500MS/s	1,125MS/s
NUMBER OF CHANNELS	2	2	4
SFDR AND HARMONICS	Same as Arbitrary		
MEMORY	Same as Arbitrary		

12.19 General Benchtop

Table 12.19 General Benchtop Specifications

Parameter	Description
INPUT VOLTAGE RANGE	100VAC to 264VAC
INPUT FREQUENCY RANGE	47Hz to 63Hz
POWER CONSUMPTION:	550W max.
EMBEDDED PC CPU MEMORY STORAGE OPERATING SYSTEM	 Intel Pentium 3MB cache, 2.20GHz 8GB (Upgradeable) 120GB (Upgradeable) Windows 10 IoT
DISPLAY	9" TFT touch LCD 1024x600
INTERFACES	
USB	Front panel 1 x USB 3 host (type A) Rear panel 2 x USB 3 host, (type A) Rear panel 1 x USB 3 device, (type C)
THUNDERBOLT (OPTIONAL)	Rear panel 1 x Thunderbolt 3
LAN (1000BASE-T)	Rear panel 1 x RJ45 1000/100/10
SFP+ (OPTIONAL, REPLACES RJ45)	Rear panel 1 x SFP+ 10G optical
GPIB (OPTIONAL)	IEEE 488.2 – GPIB
HDMI	HDMI type A
STORAGE	120GB removable
DIMENSIONS WITH FEET WITHOUT FEET	 440 X 175 x 330 mm (W x H x D) 440 X 190 x 330 mm (W x H x D)
WEIGHT WITHOUT PACKAGE SHIPPING WEIGHT	 7.5 kg 9 kg

12.20 General Desktop

Table 12.20 General Desktop Specifications

Parameter	Description
INPUT VOLTAGE RANGE	100VAC to 264VAC
INPUT FREQUENCY RANGE	47Hz to 63Hz
POWER CONSUMPTION:	550W max.
BUILT-IN PC CPU MEMORY STORAGE OPERATING SYSTEM	 Intel Pentium 3M Cache, 2.20GHz 8GB (Upgradeable) 120GB (Upgradeable) Windows 10
INTERFACES	
USB	Front panel 1 x USB 3 host (type A) Rear panel 2 x USB 3 host, (type A) Rear panel 1 x USB 3 device, (type C)
THUNDERBOLT (OPTIONAL)	Rear panel 1 x Thunderbolt 3
LAN (1000BASE-T)	Rear panel 1 x RJ45 1000/100/10
SFP+ (OPTIONAL, REPLACES RJ45)	Rear panel 1 x SFP+ 10G optical
GPIB (OPTIONAL)	IEEE 488.2 – GPIB
HDMI	HDMI type A
STORAGE	120GB removable
DIMENSIONS WITH FEET	 175 X 221 x 316 mm (W x H x D)

Parameter	Description
WITHOUT FEET	175 X 235 x 316 mm (W x H x D)
WEIGHT WITHOUT PACKAGE SHIPPING WEIGHT	 7.5 kg 9 kg

12.21 General Module

Table 12.21 General Module Specifications

Parameter	Description
INTERFACE	PXIe Gen3 x8 lanes
POWER CONSUMPTION	50W max. per slot
CURRENT CONSUMPTION	+3.3V 4A max., +12V 4A max.
DIMENSIONS	3U, 8HP PXIe (2 slots) Add 4HP (1 slot) for each AWT/MRK option

12.22 General

Table 12.22 General Specifications

Parameter	Description
TEMPERATURE OPERATING STORAGE	 0°C to +40°C -40°C to +70°C
WARM UP TIME:	15 minutes
HUMIDITY:	85% RH, non-condensing
SAFETY:	CE Marked, EC61010-1:2010
EMC:	IEC 61326-1:2013
CALIBRATION:	2 years
WARRANTY	3 years

12.23 Ordering Information Benchtop

Table 12.23 Ordering Information Benchtop

Model	Description
P1282B	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, benchtop RF AWG
P1284B	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, benchtop RF AWG
P1288B	1.25 GS/s, 16 bit, 2 GS memory, 8 channels 8 markers, benchtop RF AWG
P12812B	1.25 GS/s, 16 bit, 2 GS memory, 12 channels 12 markers, benchtop RF AWG
P2582B	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, benchtop RF AWG
P2584B	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, benchtop RF AWG
P2588B	2.5 GS/s, 16 bit, 2 GS memory, 8 channels 16 markers, benchtop RF AWG
P25812B	2.5 GS/s, 16 bit, 2 GS memory, 12 channels, 24 markers, benchtop RF AWG
P9082B	9 GS/s, 16 bit, 4 GS memory, 2 channels, 8 markers, benchtop RF AWG
P9084B	9 GS/s, 16 bit, 4 GS memory, 4 channels, 16 markers, benchtop RF AWG
P9086B	9 GS/s, 16 bit, 4 GS memory, 6 channels, 24 markers, benchtop RF AWG
P9482B	9 GS/s, 16 bit, 8 GS memory, 2 channels, 8 markers, benchtop RF AWG
P9484B	9 GS/s, 16 bit, 8 GS memory, 4 channels, 8 markers, benchtop RF AWG
P9488B	9 GS/s, 16 bit, 8 GS memory, 8 channels, 16 markers, benchtop RF AWG
P94812B	9 GS/s, 16 bit, 8 GS memory, 12 channels, 24 markers, benchtop RF AWG

12.24 Ordering Information Desktop

Table 12.24 Ordering Information Desktop

Model	Description
P1282D	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, desktop RF AWG
P1284D	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, desktop RF AWG
P1288D	1.25 GS/s, 16 bit, 2 GS memory, 8 channels, 8 markers, desktop RF AWG
P12812D	1.25 GS/s, 16 bit, 2 GS memory, 12 channels, 12 markers, desktop RF AWG
P2582D	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, desktop RF AWG
P2584D	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, desktop RF AWG
P2588D	2.5 GS/s, 16 bit, 2 GS memory, 8 channels 16 markers, desktop RF AWG
P25812D	2.5 GS/s, 16 bit, 2 GS memory, 12 channels, 24 markers, desktop RF AWG
P9082D	9 GS/s, 16 bit, 4 GS memory, 2 channels, 8 markers, desktop RF AWG
P9084D	9 GS/s, 16 bit, 4 GS memory, 4 channels, 16 markers, desktop RF AWG
P9086D	9 GS/s, 16 bit, 4 GS memory, 6 channels, 24 markers, desktop RF AWG
P9482D	9 GS/s 16 bit, 8 GS memory, 2 channels, 8 markers, desktop RF AWG
P9484D	9 GS/s 16 bit, 8 GS memory, 4 channels, 8 markers, desktop RF AWG
P9488D	9GS/s 16 bit, 8 GS memory, 8 channels, 16 markers, desktop RF AWG
P94812D	9 GS/s 16 bit, 8 GS memory, 12 channels, 24 markers, desktop RF AWG

12.25 Ordering Information Module

Table 12.25 Ordering Information Module

Model	Description
P1282M	1.25 GS/s, 16 bit, 1 GS memory, 2 channels, 4 markers, module RF AWG
P1284M	1.25 GS/s, 16 bit, 1 GS memory, 4 channels, 4 markers, module RF AWG
P2582M	2.5 GS/s, 16 bit, 2 GS memory, 2 channels, 8 markers, module RF AWG
P2584M	2.5 GS/s, 16 bit, 2 GS memory, 4 channels, 8 markers, module RF AWG
P9082M	9 GS/s, 8 bit, 4 GS memory, 2 channels, 8 markers, module RF AWG
P9482M	9 GS/s, 16 bit, 8 GS memory, 2 channels, 8 markers, module RF AWG
P9484M	9 GS/s, 16 bit, 8 GS memory, 4 channels, 8 markers, module RF AWG

12.26 Ordering Information Options

Table 12.26 Ordering Information Options

Option	Description	Model
4M1	4 GS memory	P1282y, P2582y
4M2	4 GS memory	P1284y, P2584y
4M3[2]	4 GS memory option	P1288y, P2588y, P9084y
4M4[2]	4 GS memory	P12812y, P25812y, P9086y
8M1	8 GS memory	P1282y, P2582y
8M2	8 GS memory	P1284y, P2584y, P9082y
8M3[2]	8 GS memory	P1288y, P2588y, P9084y
8M4[2]	8 GS memory	P12812y, P25812y, P9086y
16M1	16 GS memory	P9082y
16M2	16 GS memory	P9084y
16M3[2]	16 GS memory	P9086y
DO1	9 GHz BW direct output	P1282y, P2582y
DO2	9 GHz BW direct output	P1284y, P2584y, P9082y
DO3[2]	9 GHz BW direct output	P1288y, P2588y, P9084y

Option	Description	Model
DO4[2]	9 GHz BW direct output	P12812y, P25812y,P9086y
DC1	DC output for IQ baseband applications	P9482y
DC2	DC output for IQ baseband applications	P9484y
DC3[2]	DC output for IQ baseband applications	P9488y
DC4[2]	DC output for IQ baseband applications	P94812y
DJ1	Dynamic jump input, occupies an additional slot	P1282y, P2582y, P9482y
DJ2	Dynamic jump input, occupies an additional slot	P1284y, P2584y, P9082y, P9484y
DJ3[2]	Dynamic jump input, occupies an additional slot	P1288y, P2588y, P9084y, P9488y
LVTTL1	LVTTL marker output (replaces the 1.3 Vpp default markers)	P1282y, P2582y, P1284y, P2584y, P9482y, P9484y
LVTTL2	LVTTL marker output (replaces the 1.3 Vpp default markers)	P1288y, P2588y, P9084y, P9488x
LVTTL3	LVTTL marker output (replaces the 1.3 Vpp default markers)	P12812y, P25812y, P9086y, P94812y
MRK1	4 extra markers	P1282y
MRK2[2]	8 extra markers	P1288y
MRK3[2]	12 extra markers	P12812y
LTJ1	Ultra-low trigger jitter (200 ps typ.)	P1282y, P2582y, P9482y
LTJ2	Ultra-low trigger jitter (200 ps typ.)	P1284y, P2584y, P9082y, P9484y
LTJ3[2]	Ultra-low trigger jitter (200 ps typ.)	P1288y, P2588y, P9084y, P9488y
LTJ4[2]	Ultra-low trigger jitter (200 ps typ.)	P12812y, P25812y, P9086y, P94812y
G1	Low waveform granularity	P1282y, P2582y, P9482y
G2	Low waveform granularity	P1284y, P2584y, P9082y, P9484y
G3[2]	Low waveform granularity	P1288y, P2588y, P9084y, P9488y
G4[2]	Low waveform granularity	P12812y, P25812y, P9086y, P94812y
DUC	Digital up-converter	P258xy
SEC[2]	Removable SSD	All models
SSD[2]	Extra factory duplicated SSD disk for SEC	All models
TRG	Fast trigger input (50 MHz instead of 10 MHz)	All models
AWT	5.4 GS/s single, 2.7 GS/s dual channel 12 bit digitizer, occupies an additional slot	All models
STM	Up to 6 GS/s streaming varies depending model	All models
WE	1 year warranty extension	All models
PROG	FPGA programming capability with built-in demodulation and digital filters	All models
SHELL	Integration to allow simple FPGA control and programming IP (includes 50 hours support pack)	All models
PXE21100	21 slot PXIe chassis	All modules
PXE6410	6 slot PXIe chassis with an embedded PC	All modules
COM1	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 4 core, 6 MB cache, 2.2 GHz processor	
COM2	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 8 core, 12 MB cache, 2 GHz processor	
COM3	Upgrade of the PXE6410/Desktop/Benchtop to an Intel Xeon 12 core, 18 MB cache, 1.5 GHz processor	
RAM32	Upgrade to 32 GB on-board memory for the COM	
RAM64	Upgrade to 64 GB on-board memory for the COM	
RAM128	Upgrade to 128 GB on-board memory for the COM	

[1] x = Number of channels, y=M/B/D=Module/Benchtop/Desktop
[2] Only for Benchtop/Desktop

13 Appendix A. MDR Interface

The allowed voltage levels for the Mini D Ribbon (MDR) connector are 0 - 5 V (TTL) (or 0-3.3 V CMOS) and must comply with VIH=1.17 V, VIL=0.63 V levels. Voltage levels below -0.5 V and above 6 V will damage the device.

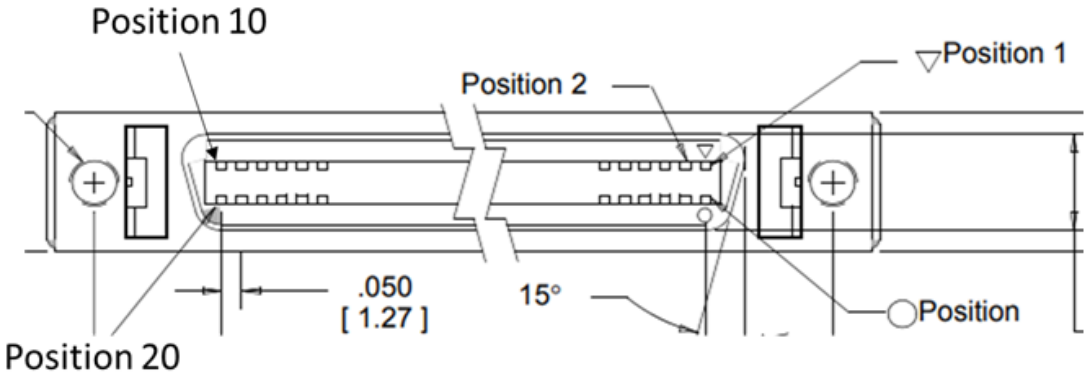

Figure 13.1 MDR Connector Pin Numbering

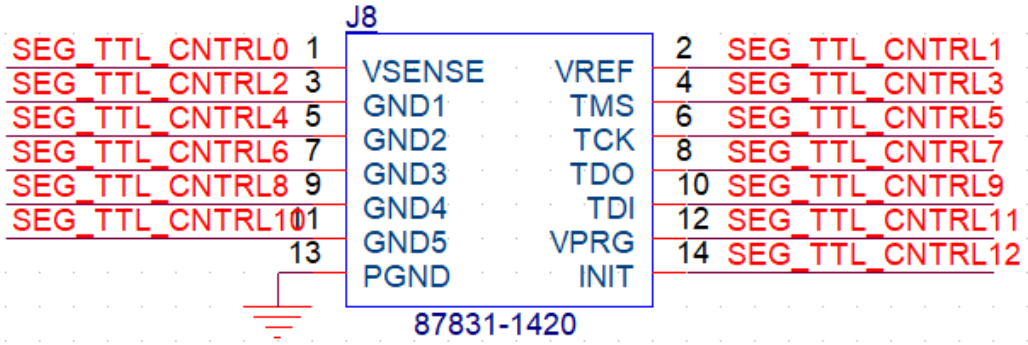

Figure 13.2 MDR Connector Pad Description

Table 13.1 MDR Connector Pin Description

Signal	Description	Pin
SEG_TTL_CNTRL0	Data LSB	1
SEG_TTL_CNTRL1	Data	2
SEG_TTL_CNTRL2	Data	3
SEG_TTL_CNTRL3	Data	4
SEG_TTL_CNTRL4	Data	5
SEG_TTL_CNTRL5	Data	6
SEG_TTL_CNTRL6	Data	7
SEG_TTL_CNTRL7	Data	8
SEG_TTL_CNTRL8	Data	9

Signal	Description	Pin
SEG_TTL_CNTRL9	Data MSB	10
SEG_TTL_CNTRL10	Channel number LSB	11
SEG_TTL_CNTRL11	Channel number MSB	12
SEG_TTL_CNTRL12	Data valid	14
GND	GND	13

14 Appendix Log File

The WDS provides a log file at C:\temp that provides all the communication between WDS and the device. If you encounter any issue, include this file in the report to Tabor support.

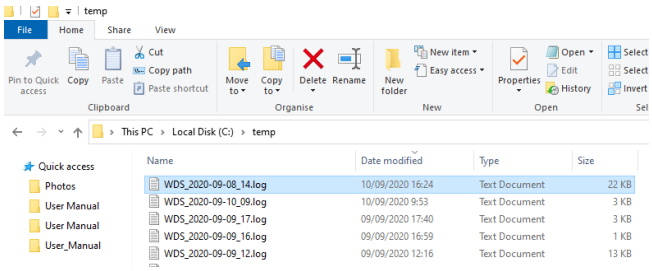

Figure 14.1 WDS Log File Folder

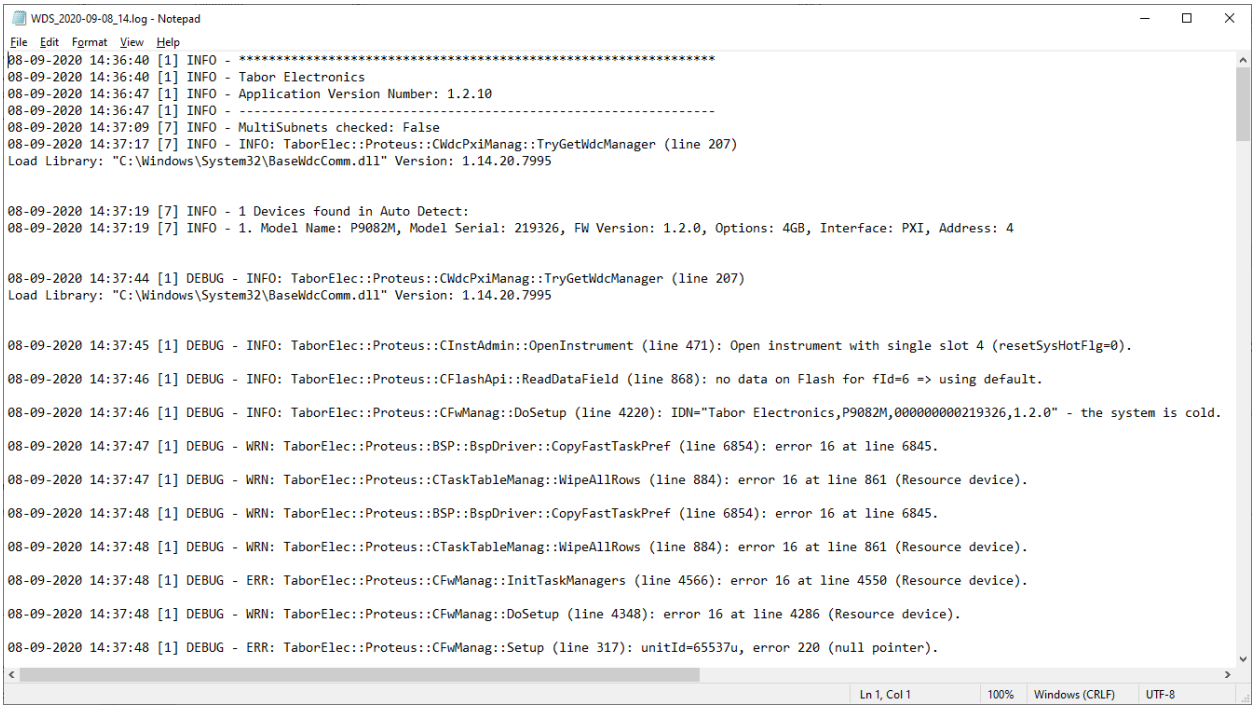

Figure 14.2 WDS Log File